Low Latency FPGA Acceleration of Market Data Feed Arbitration

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Overview

- Hardware accelerated, low latency A/B line arbitrator
  - 2 packet processing modes: low latency + high reliability
  - dynamically reconfigurable windowing
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• Multiple market data feed protocols
  – NASDAQ TotalView-ITCH
  – OPRA
  – ARCA
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• Evaluation: Xilinx Virtex-5 + Virtex-6 FPGAs
  – 10x lower latency than commercial FPGA-based solution
  – 42-56ns latency in high-reliability mode
  – 5.25-6ns latency in low-latency mode (single cycle)
Background

- **A/B line arbitration:**
  - time-critical market data
  - retransmission of missing packets too time consuming
  - receive as two redundant UDP streams (A/B feed)

- **Challenge:**
  - deal with missing and out-of-order packets through arbitration between two lines
  - need high throughput and low latency
Accelerating A/B Line Arbitration

- Simultaneous streams: low-latency + high-reliability
- Dynamically reconfigurable:
  - 3 windowing modes
  - adapt to changes in downstream applications
Optimisations

- Network level operation
  - also deals with general network traffic
- Customisable and extensible
  - support various protocols, connectors
  - configurable datapath width, stored packet size/num

![Time-based windowing](image)

![Count-based windowing](image)
Implementation Results

- Implementation for three protocols
  - NASDAQ TotalView-ITCH
  - OPRA
  - ARCA
- Throughput > 20 Gbps
- 10x lower latency than commercial FPGA solution
- Xilinx Virtex-5
  - test with real market data over network card (2x10Gbps)
- Xilinx Virtex-6
  - NASDAQ TotalView-ITCH
    - 6ns (low-latency), 56ns (high-reliability)
  - OPRA and ARCA:
    - 5.25ns (low-latency), 42ns (high-reliability)
Summary

- Hardware accelerated, low latency A/B line arbitrator
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  - dynamically reconfigurable windowing

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