

Exercise 3

1 MRMW Atomic Register

In the shared-memory model, implement a MRMW atomic R/W register using MRSW atomic R/W registers. Idea: every writer uses a separate pair of registers (τ, x) to write, and τ is implemented as a vector clock.

2 Perfect Failure Detector

- a) Assume that a bound Δ on message delay is known and holds always. Design a perfect failure detector $\mathcal{D} \in \mathcal{P}$.
- b) Assume that a bound Δ on message delay exists, but is not known to the protocol designer, and that the bound holds only after some “global stabilization time” t_Δ . Design an eventually perfect failure detector $\mathcal{D} \in \diamond\mathcal{P}$.