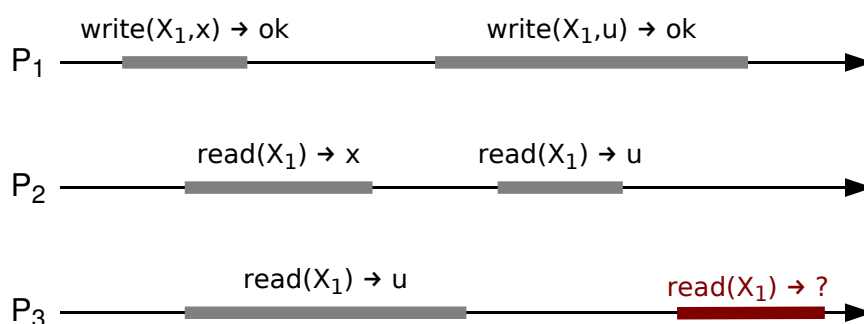


Exercise 3

1 A MRSW Register

There are servers P_1, P_2, P_3 and one MRSW register X_1 with arbitrary domain \mathcal{D} , to which P_1 may write and from which all servers may read. Consider the following execution with $x, u \in \mathcal{D}$:



What return value(s) may P_3 obtain from its second *read* operation, if the register has safe, regular, or atomic semantics? Justify your answer.

2 Multi-Reader from Single-Reader Registers

Consider the following implementation of a MRSW register R , with operations *READ* and *WRITE*, from n SRSW registers r_1, \dots, r_n , with operations *read* and *write*. This is the algorithm for P_i :

<p><i>WRITE</i>(R, v):</p> <p style="padding-left: 2em;">for $j = 1, \dots, n$ do</p> <p style="padding-left: 4em;"><i>write</i>(r_j, v)</p> <p style="padding-left: 2em;">return ok</p>	<p><i>READ</i>(R):</p> <p style="padding-left: 2em;">return <i>read</i>(r_i)</p>
--	---

- a) Let r_1, \dots, r_n be safe binary SRSW registers. Prove that R is a safe binary MRSW register.
- b) If we replace the n safe SRSW registers r_1, \dots, r_n with an array of *regular binary* SRSW registers, does the algorithm implement a *regular binary* MRSW register?
- c) If we replace the n safe SRSW registers r_1, \dots, r_n with an array of *regular multi-valued* SRSW registers, does the algorithm implement a *regular multi-valued* MRSW register?