

# Design and Verification Methodology of Modern High-Speed Switches

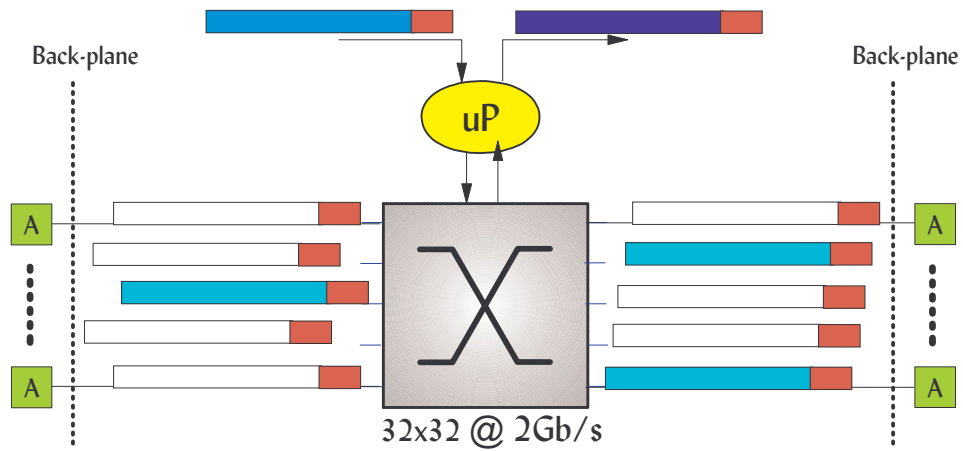
- A C++ Modeling Approach -

F. Abel - IBM Zurich Research Lab.

## Outline

- ▶ Packet-Routing Switch Overview
- ▶ Design Methodology
  - C++ Behavioral Model
- ▶ Principles of Validation
  - Unified Simulation Environment
- ▶ Results
- ▶ Conclusions

# Packet-Routing Switch - Overview



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## Outline

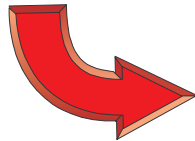


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## Design Complexity

- ▶ High degree of parallelism
- ▶ Short clock cycle (4ns)
- ▶ OEM oriented
  - Four expansion modes
  - Multiple configurations
- ▶ Time 2 market, Cost ...



## Requirements Design & Validation Environment

- ▶ Fast design exploration
- ▶ Continuous refinement
- ▶ Fast simulation/validation

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## C++ Based Design Methodology

### Disadvantages

- Switch design
  - Manual translation in HDL
- Testcases/Testbenches
  - Manual conversion
- Maintain 2 models

### Decisions

- Automated translation
  - "stylized VHDL" coding
- Unified environment
  - Used at all levels
- C++ clock accurate model

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## C++ Behavior Model - Entity Declaration

```
entity(InpCtrl)
// Itf with the Application Registers (ARG)
input      ( boolean, ARG_StandbyReset );
input      ( boolean, ARG_MasterPort );
input      ( boolean, ARG_ControllerEnable );
inputArray ( boolean, ARG_OQueueEnable, 32 );
inputArray ( boolean, ARG_BMFilterMask, 32 );
...
// Itf with Input Frame Processing (IFRAM)
input      ( boolean, IFRAM_DiscardThisCell );
input      ( int,     IFRAM_RXCountIn );
input      ( int,     IFRAM_RowCountIn );
...
// Itf with the On Chip Monitor Registers (ORG)
output     ( boolean, ICTRL_NoAddrError );
...
// Itf with Packet Memory (PktMem)
output     ( boolean, ICTRL_InsAddr );
...
// Itf with On Chip Monitor (OCM)
// For beh model only. Used to gather some stat.
input      ( p_oGlobalChipData, ARG_GlobData );
};
```

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```
architecture(default, InpCtrl)
```

```
...
boolean    Receiving;
boolean    IdleCell;
byte       Qualifier;
boolean    ASAINvalid;
uLong      BMHeader;
...
```

```
void ClockTick(int itfnr) { ..... wait until clock'event and clock='1';
...
int    ByteCounter;
...
if (sread(ARG_StandbyReset) == TRUE) { // Reset Sequence
...
return;
}
...
ByteCounter = sread(IFRAM_RXCountIn);
if ((RowCounter == 0) && sread(ARG_MasterPort)) {
...
swrite(ICTRL_NoAddrError) = TRUE;
...
}
}
```

```
end_architecture(default, InpCtrl);
select_architecture(default, InpCtrl);
```

## C++ Behavior Model - Body of the Process


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```
else if (Qualifier != 0xCC) {
    if (ASAINvalid == TRUE) {
        if (DataCell == TRUE) {
            swrite(CTRL_NoAddrError) = TRUE;
            Error("No ASA Address available!");
        }
    }
}
//
//
}
...
}
...
}
end_architecture(default, InpCtrl);
select_architecture(default, InpCtrl);
```

11) {

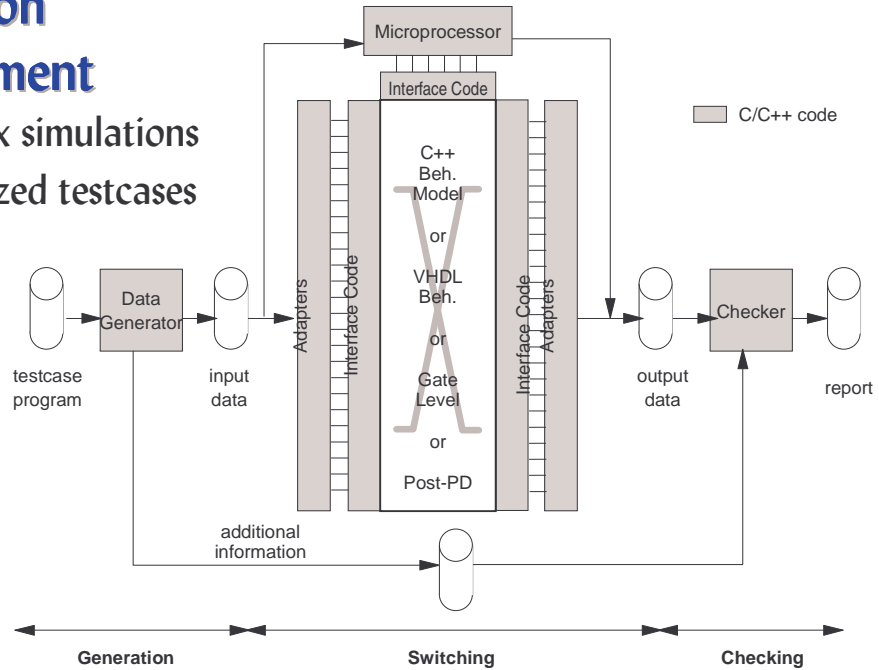
# Manual Translation

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## Validation Environment

- Black-box simulations
- Randomized testcases



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## Results (1/3)

- ▶ Simulation Time : RS/6000 - 375MHz processor - 2GB of memory

	C++ Beh.	VHDL/RTL	Gate Level	
tc_connect	time	43s	12'52s	9H55'47s
	speed	277	15.5	0.33

Simulation time and speed (in clock cycles/second)



- ▶ Validation Environment

- 160.000 lines of C/C++ ~ 5.000 lines of Shell scripts
  - Resources = 1 Architect + 1 Software Engineer
- 100 testcases
  - Resources = 5 to 8 Testcase writers
  - Regression = 5000 testcase runs

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## Results (2/3)

- ▶ Test coverage & Randomized testcases
- ▶ Distributed Regression
  - 50 workstations => 5000 testcase runs in 12 hours
- ▶ Simulation Processes

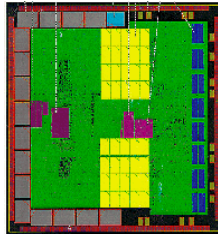
	C++ Beh.	VHDL/RTL	Gate Level
1 PSR64G chip	6.8	150	650
2 PRS64G chips	10	200	913

Size of the simulation process (in MB)

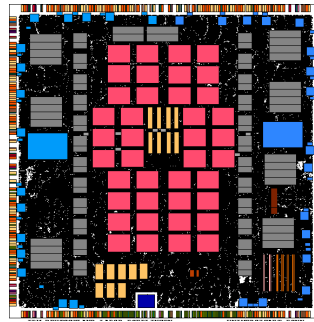
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## Results (3/3)

- ▶ 2 Successful ASIC designs : PRS28.4G & PRS64G
  - Fast simulation time
  - Pin-out simulation & Randomized testcases
  - Quality of the C++ to VHDL translation
- ▶ Design cycle # 18 months



PRS28.4G (16x16)



PRS64G (32x32)

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## Conclusions

- ▶ Most of the HW design and verification of a packet-routing switch can be handled at a C++ level
- ▶ C++ to model hardware
  - High design productivity and fast simulation
  - Faster simulation => Significant reduction of the design cycle
  - + More time for architectural investigations and optimizations
- ▶ Unified Validation Environment
  - C++ based => Faster to develop and execute
  - Faster VHDL validation => Env. is ready and debugged
  - + More time for synthesis and real error corrections
- ▶ Directions for Future Research
  - + Hardware synthesis directly from C++

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→ PRS28.4G :

<http://www.chips.ibm.com/products/commun/documents/prs28.pub.pdf>

→ PRS64G :

<http://www.chips.ibm.com/products/commun/documents/prs64.pub.pdf>

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