ASAP 2014 Program

Wednesday

9:00 – 9:30 Opening Remarks
9:30 – 10:30 Keynote 1

Oskar Mencer. Computing in Space

10:30 – 11:00 Break
11:00 – 12:50 Session 1: Hardware Accelerators I

Regular Paper:

119 Kabilay Atasu. Resource-Efficient Regular Expression Matching Architecture for Text Analytics
18 Iñaki Bildosola, Unai Martinez-Corral and Koldo Basterretxea. Scalable SVD Unit for Fast Processing of Large LSE Problems on FPGAs

Short Paper:

43 Michael Gautschi, Michael Muehlberghuber, Andreas Traber, Sven Stucki, Matthias Baer, Renzo Andri, Luca Benini, Beat Muheim and Hubert Kaeusi. SIR10US: A Tightly-Coupled Elliptic-Curve Cryptography Co-Processor for the OpenRISC
97 Mohammad Badawi, Ahmed Hemani and Zhonghai Lu. Customizable Coarse-grained Energy-efficient Reconfigurable Packet Processing Architecture
45 Stewart Denholm, Hiroaki Inoue, Takashi Takenaka and Wayne Luk. Low Latency FPGA Acceleration of Market Data Feed Arbitration

12:50 – 14:20 Lunch Break
14:20 – 15:30 Session 2: Computer Arithmetric

Regular Papers

109 Florent de Dinechin, Albdelbassat Massouri and Matei Istoan. Sum-of-Product Architectures Computing Just Right
68 Hamad Alrimeih and Daler Rakhmatov. Pipelined Modular Multiplier Supporting Multiple Standard Prime Fields

Short Papers
Karim Bigou and Arnaud Tisserand. RNS Modular Multiplication through Reduced Base Extensions

Mioara Joldes, Jean-Michel Muller and Valentina Popescu. On the computation of the reciprocal of floating point expansions using an adapted Newton-Raphson iteration

15:30 – 16:30 Poster Session I Break

Anro Altamimi, Daler Rakhmatov and Michael McGuire. Polar Baseband Receiver for Low-End WLAN

Yun-Nan Chang and Ting-Chi Tong. Design of a 2D graphics front-end rendering processor

Michael Hall and Roger Chamberlain. Performance Modeling of Virtualized Custom Logic Computations

Ali Hayek. HiCore1: “Safety on a Chip” Turnkey Solution for Industrial Control

Mehdi Modarressi and Hamid Sarbazi-Azad. A Reconfigurable Network-on-chip for Heterogeneous Many-core CMPs in the Dark Silicon Era

Simon Pontié and Paolo Maistri. Randomized Windows for a Secure Crypto-Processor on Elliptic Curves

Mariagiovanna Sami and Gianluca Palermo. Virtual semi-concurrent self-checking for heterogeneous MPSoC architectures

Hao Xiao, Tsuyoshi Isshiki, Dongju Li, Hiroaki Kunieda and Guanyu Zhu. Distributed Synchronization for Message-passing based Embedded Multiprocessors

16:30 – 18:00 Session 3: Performance and Power Analysis

Regular Papers:

Lin Ma, Roger Chamberlain and Kunal Agrawal. Performance Modeling for Highly-threaded Many-core GPUs

Heiner Giefers, Raphael Polig and Christoph Hagleitner. Analyzing the energy-efficiency of dense linear algebra kernels by power-profiling a hybrid CPU/FPGA system

Nathaniel Conos, Saro Meguerdichian and Miodrag Potkonjak. Coordinated and Adaptive Power Gating and Dynamic Voltage Scaling for Energy Minimization

Short Papers

Ahmad Lashgar and Amirali Baniasadi. A Case Against Small Data Types
Thursday

9:00 – 9:30  Announcements, Best Paper Awards, Introduction to ASAP 2015

9:30 – 10:30  Keynote 2

Jeff Stuecheli. Open Innovation with POWER8

10:30 – 11:00  Break

11:00 – 12:50  Session 4: Architectures I

Regular Papers:

60  Francesco Conti, Chuck Pilkington, Andrea Marongiu and Luca Benini. He-P2012: Architectural Heterogeneity Exploration on a Scalable Many-Core Platform

48  Hamed Tabkhi, Robert Bushey and Gunar Schirmer. Function-Level Processor (FLP): Raising Efficiency by Operating at Function Granularity for Market-Oriented MPSoCs

73  Waqar Hussain, Roberto Airoldi, Henry Hoffmann, Tapani Ahonen and Jari Nurmi. Design of an Accelerator-Rich Architecture by Integrating Multiple Heterogeneous Coarse Grain Reconfigurable Arrays over a Network-on-Chip

120  Taimour Wehbe and Xiaofang Maggie Wang. Fault-tolerant on-chip networking through adaptive routing and dynamic partial reconfiguration

Short Papers

92  Ruan de Clercq, Dries Schellekens, Frank Piessens and Ingrid Verbauwhede. Secure Interrupts on low-end microcontrollers

12:50 – 14:20  Lunch Break

14:20 – 15:30  Session 5: Programming

Regular Papers:

72  Konstantinos Krommydas, Wu-Chun Feng, Muhsen Owaida, Christos D. Antonopoulos and Nikolaos Bellas. On the Portability of OpenCL Dwarfs on Fixed and Reconfigurable Parallel Platforms

86  Edoardo Paone, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano and Davide Gadioli. Evaluating Orthogonality between Application Auto-Tuning and Run-Time Resource Management for Adaptive OpenCL Applications

Short Papers

35  Thomas Peyret, Gwenole Corre, Mathieu Thevenin, Kevin Martin and Philippe Coussy. Efficient Application Mapping on CGRAs based on Backward Simultaneous Scheduling/Binding and Dynamic Graph Transformations
Moritz Schmid, Alexandru Tanase, Vivek Singh Bhadouria, Frank Hannig, Jürgen Teich and Dibyendu Ghoshal. Domain-Specific Augmentations for High-Level Synthesis

15:30 – 16:30 Poster Session II Break

Junyi Han, Bruce D'Amora, Bob Danani, Adel Salhi and John Brooke. Virtual science on the move: interactive access to simulations on supercomputers

Keerthan Jaic, Melissa Smith and Nilim Sarma. A Practical Network Intrusion Detection System for Inline FPGAs on 10GbE Network Adapters

Yanhua Li, Youhui Zhang, Jianfeng Yang, Wayne Luk, Guangwen Yang and Weiming Zheng. An Approach of Processor-Core Customization forStencil Computation

Yongchao Liu and Bertil Schmidt. SWAPHI: Smith-Waterman Protein Database Search on Xeon Phi Coprocessors

Kevin S. H. Ong, Suhaib A. Fahmy and Keck-Voon Ling. A Scalable and Compact Systolic Architecture for Linear Solvers


Tomohiro Ueno, Ryo Ito, Kentaro Sano and Satoru Yamamoto. Bandwidth Compression of Multiple Numerical Data Streams for High Performance Custom Computing

Shizhen Xu, Xiaomeng Huang, Yan Zhang, Yong Hu and Guangwen Yang. A Customized GPU Acceleration of the Princeton Ocean Model

16:30 – 18:00 Session 6: Hardware Accelerators II

Regular Papers:

Ce Guo, Wayne Luk and Stephen Weston. Pipelined Reconfigurable Accelerator for Ordinal Pattern Encoding

Janarbek Matai, Joo-Young Kim and Ryan Kastner. Energy Efficient Canonical Huffman Encoding

Zhenzhi Wu and Dake Liu. Flexible Multistandard FEC Processor Design With ASIP Methodology

Short Papers

Kevin Cushon, Saied Hemati, Shie Mannor and Warren Gross. Energy-Efficient Gear-Shift LDPC Decoders
Friday

9:00 – 9:10  Announcements
9:10 – 10:10  Keynote 3

Onur Mutlu. Rethinking Memory System Design for Data-Intensive Computing

10:10 – 11:00  Session 7: Memory

Regular Papers:
54  Christian Pinto and Luca Benini. Exploring DMA-assisted Prefetching strategies for Software Caches on Multicore Clusters

11:00 – 11:30  Break

11:30 – 13:00  Session 8: Architectures II

Regular Papers:
31  Tassadaq Hussain, Oscar Palomar, Osman Unsal, Adrian Cristal, Eduard Ayguade and Mateo Valero. PVMC: Programmable Vector Memory Controller
106  Berkin Akin, Franz Franchetti and James Hoe. Understanding the Design Space of DRAM-Optimized Hardware FFT Accelerators
89  Deepak Gangadharan, Samarjit Chakraborty and Jürgen Teich. Quality-aware Video Decoding on Thermally-constrained MPSoC Platforms

Short Papers

22  Joao Andrade, Frederico Pratas, Gabriel Falcao, Vitor Silva and Leonel Sousa. Combining Flexibility with Low Power: Dataflow and Widepipeline LDPC Decoding Engines in the Gbit/s Era