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TDM Based Memristive Triplet-STDP

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INTRODUCTION:

- Spike Timing Dependent Plasticity rules are subset of Synaptic Plasticity rules that governs weight modifications based upon spike timing difference between firing of pre and post neurons across synapses. Synaptic Plasticity rules accounts for uncorrelated activities across synapses to modify and also to compete with each other to get them weakened or strengthened.

- Our work presents an analog implementation of T-STDP (Triplet-based Spike timing dependent plasticity) circuit that emulates the BCM (Bienenstock-Cooper-Munro) characteristics and is capable of direct integration with silicon Neurons.

- The circuit uses a memristor whose conductance gets modulated based on potentiation or depression according to the time difference between the triplets of spiking patterns viz. Pre-Post-Pre or Post-Pre-Post. Accordingly, the circuit eliminates the problem of charge leakage and poor retention in conventional capacitor-based T-STDP circuit.

- Further, all required signals such as Post(n-1) or Pre(n-1) are generated within the circuit itself eliminating the requirement of external circuitry as required in conventional T-STDP circuit.

1. Pair-Based STDP (P-STDP):

- Most commonly used STDP protocol, extensively used in electro-physiological experiments, mathematically mapped as:

$$\Delta w = \begin{cases} A^{+} e^{\left(\frac{-\Delta t}{\tau_{+}}\right)} & , if \;\; \Delta t > 0 \quad (1) \\ -A^{-} e^{\left(\frac{\Delta t}{\tau_{-}}\right)} & , if \;\; \Delta t \leq 0 \end{cases}$$

where, Δt represents timing difference between single pair of post and pre synaptic firings, given as $t_{post} - t_{pre}$. Weight will potentiate if pre-synaptic firing occurs in specific window time (τ+) before the post-synaptic firing. Otherwise, Depression in weight occurs if pre-synaptic firing occurs within specific window time (τ−) after the post-synaptic firing. Timing difference in Pre and post firings, their temporal order and amplitudes $A^{+} and\, A^{-}$ governs the amount of weight change.

2. Triplet-Based STDP (T-STDP):

- In T-STDP, Synaptic weight changes based upon the timing difference among triplet combination of spikes. It often works with triplet or higher order temporal spiking patterns and is mathematically modeled as:

$$\Delta w = \begin{cases} A_2^{+} e^{\left(\frac{-\Delta t_1}{\tau_{+}}\right)} + A_3^{+} e^{\left(\frac{-\Delta t_2}{\tau_y}\right)} e^{\left(\frac{-\Delta t_1}{\tau_{+}}\right)} & if \; t = t_{post} \quad (2) \\ -A_2^{-} e^{\left(\frac{\Delta t_1}{\tau_{-}}\right)} - A_3^{-} e^{\left(\frac{-\Delta t_3}{\tau_x}\right)} e^{\left(\frac{\Delta t_1}{\tau_{-}}\right)} & if \; t = t_{pre} \end{cases}$$

Potentiation in weight happens if post-synaptic spike occurs; with $A_2^{+} and\, A_3^{+}$ as triplet term potentiation amplitude parameters whereas depression happens if there occurs pre-synaptic firing with $A_2^{-} and\, A_3^{-}$ as triplet term depression amplitude parameters. $\Delta t_1 = t_{post}(n) - t_{pre}(n)$ corresponds to timing difference between pre and its next successive post spike; $\Delta t_2 = t_{post}(n) - t_{post}(n-1)$ corresponds to timing difference between immediate successive post spikes and $\Delta t_3 = t_{pre}(n) - t_{pre}(n-1)$ corresponds to timing difference between immediate successive pre spikes. τ_{+} and τ_y are the time constants for potentiation while τ_{-} and τ_x the same for depression.

Benefits of TSTDP Over PSTDP:

- TSTDP accounts absence in potentiation at low pre-synaptic firing rate & vice -versa.
- Imbibe BCM characteristics that maps learning behavior under pre & post firing following possionian trains.
- *Our Proposed work can be easily integrated with silicon neurons, eliminating requirement of additional circuitry for holding the previous spikes to vary the synaptic weights based on time difference and alleviates the problem of charge leakage and poor charge retention[2].*

Time Multiplexed Memristive T-STDP Architecture

- Conceptual block is shown wherein pre-neuron is connected to post-neuron through pre-neuron & post-neuron interface circuitry as follows.
- Each time-frame is divided into 5-time-slots where first one is used for direct communication for previous neuron spikes are passed to post neuron.
- The remaining 4 slots are used to implement T-STDP behavior i.e. to implement each fours terms in eq-2 and change the synaptic weight accordingly.
- The behavior required at two ends of the memristor i.e. between pre- and post-neuron is different from each other at these four slots.

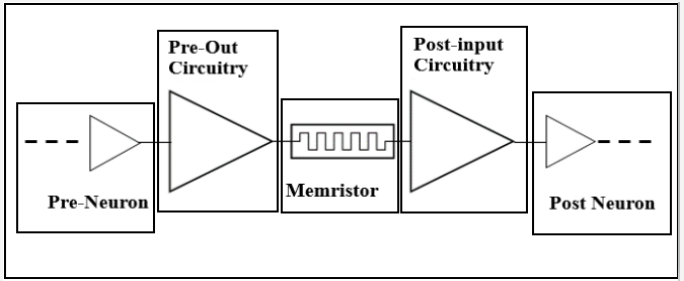


Fig. 1. Block level view of connections between pre neuron, synapse (as memristor) and post neuron.

Pre-Out Circuitry Explanation:

- The five timeslots used in one time-frame for the output of pre-neuron are COM, RES-LTD1, RES-LTD2, LTP1 & LTP2.
- The neuron will send out spike in COM timeslot with an V amplitude, fixed between Vth/2 and Vth (Vth is memristor's threshold) in such a way that single LTP1/2 pulse can't change the memristor's conductance but a cumulative application of LTP1/2 and a -V pulse at other end can change the memristor's conductance as net voltage across memristor's end exceeds the threshold voltage.
- Pre-neuron spiking in COM timeslots will induce the pulses of decaying width in LTP1 timeslot and similarly if post-neuron spikes in COM timeslot will induce the pulses of decaying width in LTP2 timeslot.
- Only if the other end of memristor is at -V level during LTP1 and LTP2 slots, which in turn reflects RES-LTP1 and RES-LTP2 time-slots for input of post neuron (discussed next) can potentiate the memristor/synapse. Also, if pre-neuron spikes in COM timeslot, it will also induce -V level in RES-LTD1 & RES-LTD2, otherwise it stays at 0.
- The time-slot LTP2 with appropriate condition in RES-LTP2 (mentioned above) reflects the first term of potentiation part in TSTDP equation and similarly LTP1 with appropriate condition in RES-LTP1 reflects the second term of potentiation part of TSTDP equation.

Post-In Circuitry Explanation:

- The five timeslots used in one time-frame for the input of post-neuron are COM, LTD1, LTD2, RES-LTP1 & RES-LTP2
- The post-neuron will receive stimuli spike with an amplitude V in the COM time-slot from pre-neuron through memristor. COM is only timeslot during which post neuron receive spikes.
- If the post-neuron spikes in the COM timeslot, it causes -V voltage at neuron's output in RES-LTP1 & RES-LTP2 timeslots, causing the LTP-1 & LTP-2 at the post-neuron output to potentiate the synapse or memristor, Otherwise the output falls or stays at a 0 during RES-LTP1 & RES-LTP2.
- If the Post-neuron provided a spike in the COM timeslot, pulses of decaying width will be induced in LTD-1 timeslot, while Pre-neuron spikes during COM will generate the pulses of decaying width in LTD-2.
- Only, if the other end of memristor (Pre-out circuitry) is at -V in LTD-1 & LTD-2 slots which in-turn reflects the RES-LTD1 & RES-LTD2 for Pre-out neuron circuitry time-slots would be able to create depression.
- The time-slot LTD2 with appropriate condition in RES-LTD2 (mentioned above) reflects the first term of depression part in TSTDP equation and similarly LTD1 with appropriate condition in RES-LTD1 reflects the second term of depression part of TSTDP equation.

- All the sub-circuitry for pre-neuron output circuitry that does particular functionalities in the COM, RES-LTD1, RES-LTD2, LTP1 & LTP2 are multiplexed using transmission gates which are controlled by COM, RES-LTD1, RES-LTD2, LTP1 & LTP2 as control signals and then output is directly fed to the top electrode of memristor.

- Similarly, all the sub-circuitry for post-neuron input circuitry that does specific functions in the COM, LTD1, LTD2, RES-LTP1 & RES-LTP2 are multiplexed using transmission gates which are controlled by COM, LTD1, LTD2, RES-LTP1 & RES-LTP2 as control signals is then directly fed to bottom electrode of memristor.

- Conductance of the memristor is used to really interpret the weight change correctly. when the conductance of memristor enhances, it is shown as potentiation of synapse while when it reduces, it can be interpreted as depotentiation or depression.

CIRCUIT DIAGRAMS:

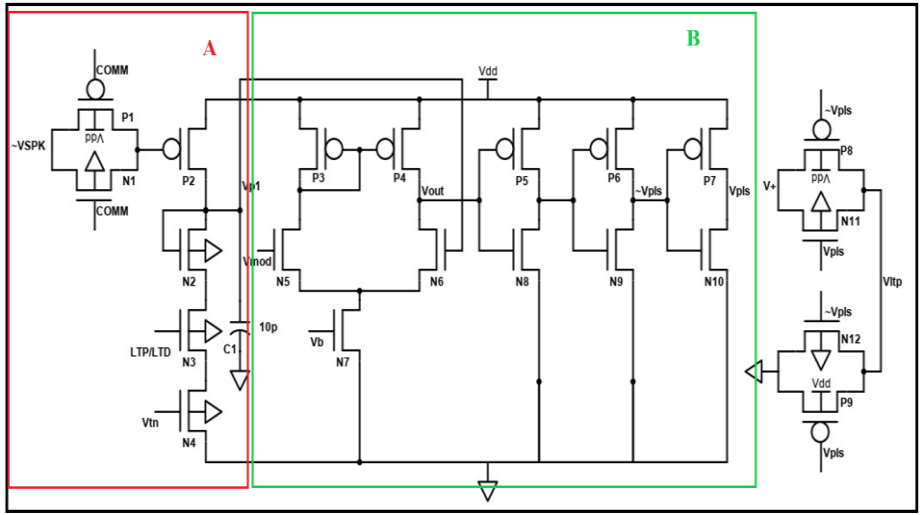


Fig. 2. Circuit diagram for the LTD/LTP blocks: (A) Linearly decaying window generator (B) Pulse Width Modulator

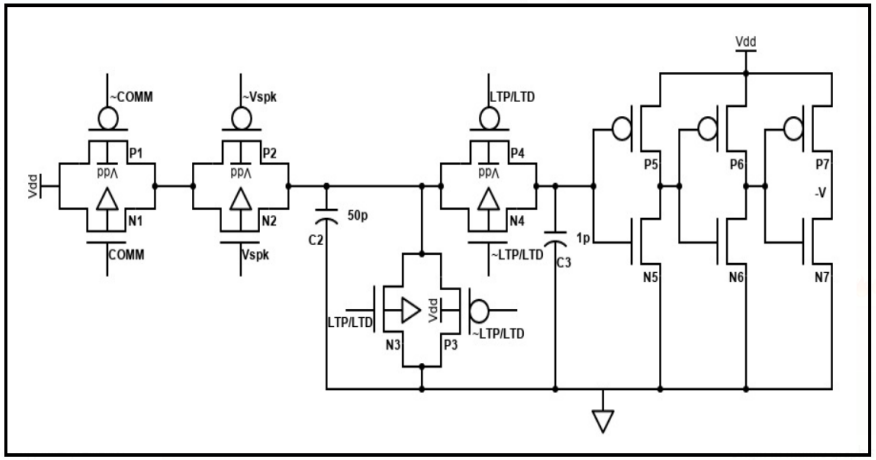
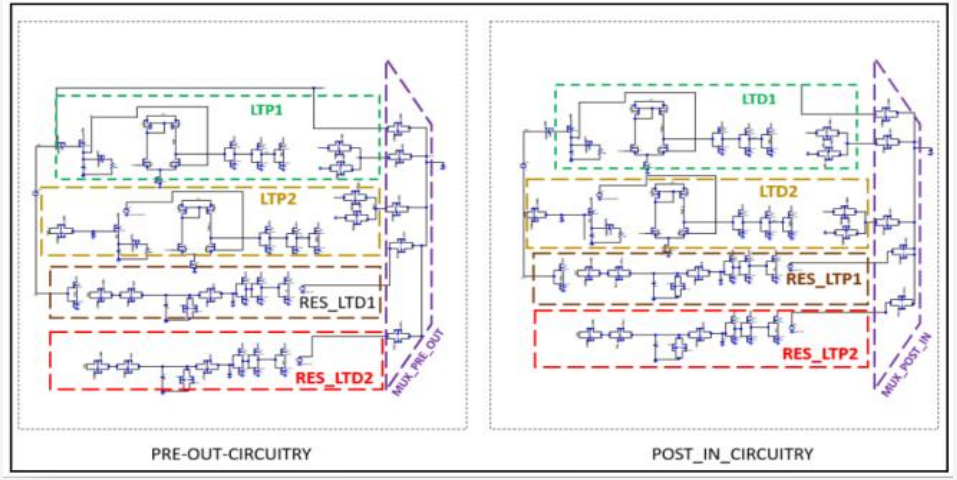


Fig. 3. Circuit for RESPONSE(RES) block that generates "gnd or -V" to support depression/potentiation

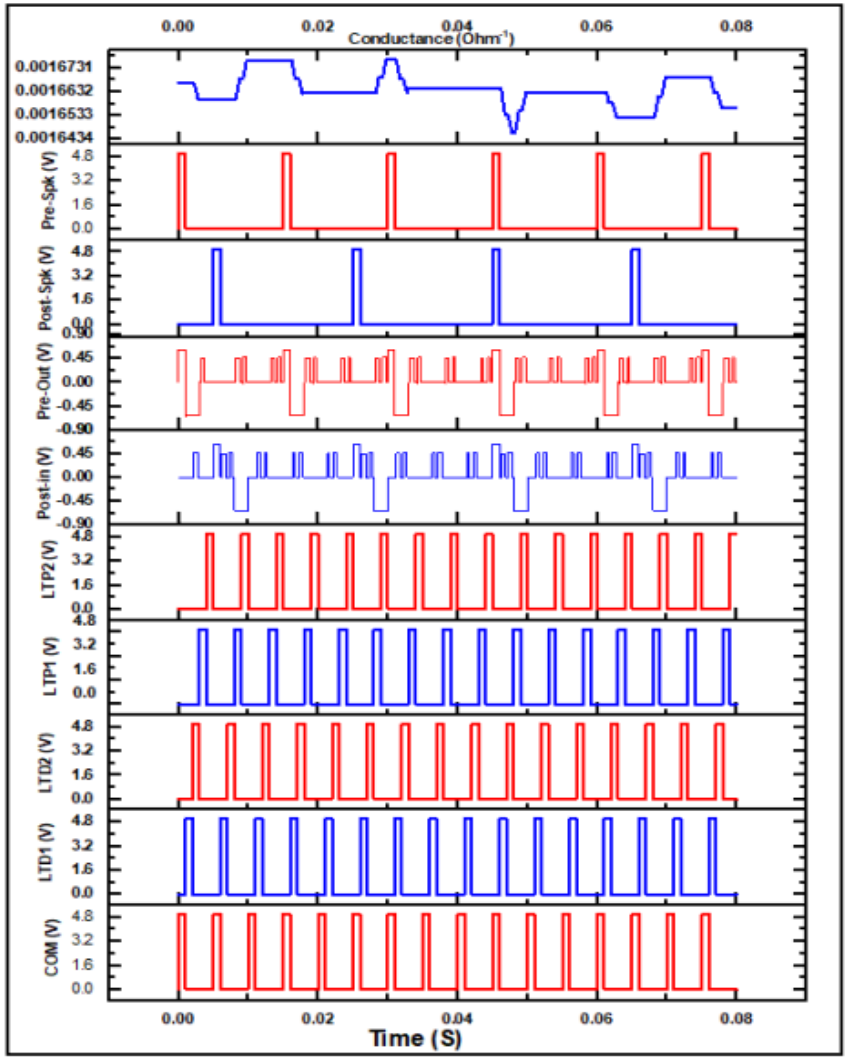
Fig. 4. Top Level View of Pre-Out circuit and Post-in Circuitry.



OUTPUTS:

- Simulation Outputs showing Changes in “Conductance across memristor” (first trace), in response to a sequence of Pre and Post Synaptic spikes(second & third trace respectively).
- Pre-out and Post-in circuitry outputs which are multiplexed outputs of various time frames described in previous slides(as shown in fourth & fifth trace respectively)
- While COM, LTD1, LTD2, LTP1 & LTP2 are various source voltage turned on during respective time intervals to address the spiking, depression and potentiation (shown in last 5 traces from 10th to 5th).

Fig. 5. Simulation results for the entire TSTDP circuit.



BCM Behavior:

- The crucial advantage of TSTDP is to mimic the BCM learning behavior, which can help in addressing the classification problems due to its characteristic rate-based rule feature under Poissonion spike trains.

- The poissonian spikes are generated through MATLAB and used as Vpre and Vpost spikes in the simulation such that λ=ρ(Pre)/ρ(Post)=1. The collected rate of change of conductance across memristor for various mean frequency Poisson spike trains are used to plot Fig. 6 in Origin tool with 2nd order curve fit.

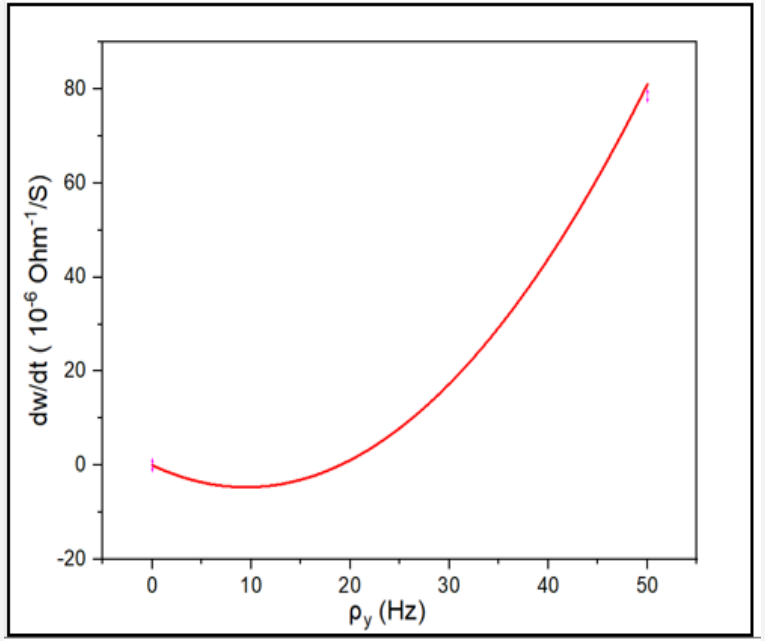


Fig. 6. Showing BCM behavior (procedure followed as mentioned in [1], but ρ_y as post-synaptic firing or spikes per sec), i.e., plot for instantaneous synaptic weight change as a function of the post spiking frequency for the proposed circuitry

CONCLUSION:

- The Simulation results show that the proposed circuit is able to implement T-STDP, retaining the crucial advantages that it provides over P-STDP, without the requirement of additional circuitry to generate Post(n-1) and Pre(n-1).
- Capacity to hold the intermediate charge level during depression or potentiation and ability to mimic the BCM behavior upon proper tuning of parameters are two important characteristics required by a T-STDP circuit. The proposed memristor based TSTDP circuit has solved the issue of charge leakage without compromising storage of the multiple levels of synaptic weights and imbibed the BCM behavior.
- Another major benefit of this TDM implementation for TSTDP is that simulation results are well comparable with real biological time.

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