T1: AI Chiplet and Emerging Hardware (Location: Aisle 26)			
T1.1	Nan	Wu	Infusing Intelligence for Automatic, Scalable, and Agile Hardware Development
T1.2	Seunghyun	Moon	Multipurpose Deep-Learning Accelerator With Reduction of Storage, Logic, and Latency Waste
T1.3	Zhenyu	Wang	HISIM: Heterogeneous Integration Simulator with 2.5D/3D Interconnect Modeling
T1.4	Ilknur	Mustafazade	Clustering and Allocation of Spiking Neural Networks on Neuromorphic Architecture
T1.5	Yunxiang	Zhang	Towards Versatile Multiplierless Deep Learning Paradigm
T1.6	Rahul	Sreekumar	EASI-CiM: Event-Driven Asynchronous Stream-based Image Classifier with Compute-in-Memory kernels
T1.7	Erik Jens	Loscalzo	Power Management for Multi-Chiplet Designs with Package Integrated Voltage Regulators
T1.8	Abdullah	Sahruri	A Neuromorphic 32-bit Arithmetic Logic Unit Based on High Fan-in Differential Capacitive Threshold-Logic Gates
T1.9	Anupreetham		Algorithm-hardware co-design of streamlined approximation aware SNN accelerator in Intel 16 CMOS
T1.10	Jared	Baumann	FSHMEM: Scaling Partitioned Global Address Space for Large-Scale AI Acceleration
T1.11	Vinod	Jacob	Efficient Compute-In-Memory in Non-Volatile Voltage-Controlled MRAM
T1.12	Harideep	Nair	Cortical Columns Computing Systems (C3S): Towards a Silicon Neocortex for AI Compute
T1.13	Purab	Sutradhar	MemAI: A Multi-chipset-based Scalable Memory-centric System for Distributed Processing of Large-scale and Generative AI Algorithms

T2: AI Algorithms (Location: Aisle 26)			
T2.1	Zhenyu	Liu	Non-Uniform Noise Injection for Enhancing DNN Adversarial Robustness and Efficiency
T2.2	Ertza	Warraich	Robust and Tail-Optimal AllReduce for Distributed Deep Learning in the Cloud
T2.3	Shurui	Li	Weight Pooling: A Compression Technique for Alleviating Memory Bottlenecks in Neural Networks
T2.4	Reza	Sadeghi	Genetic Support Vector Data Description
T2.5	Nastaran	Darabi	STARNet: Sensor Trustworthiness and Anomaly Recognition via Approximated Likelihood Regret for Robust Edge Autonomy
T2.6	Mohanad	Odema	Inter-Layer Scheduling Space Exploration for Multi-model Inference on Heterogeneous Chiplets
T2.7	Zishen	Wan	Towards Bit Error Robust Energy-Efficient Autonomous Systems
T2.8	Jeff	Wu	Graph neural networks for analog interconnect capacitance estimation
T2.9	Frederick	Rizk	Unveiling the Enigma of MAGAN: Navigating into Generative Adversarial Networks' Hidden Latent Space
T2.10	Hadjer	Benmeziane	Are Large Language Models Good Neural Architecture Generators?
T2.11	Mohammed Nowaz Rabbani	Chowdhury	Coarser-grained Structured Pruning: Pruning Experts in Mixture-of-Experts with Theoretical Performance Guarantee

T3: AI Applications (Location: Cafeteria)			
T3.1	MSVPJ	Sathvik	GoogleGPT: Knowledge Infusion Architecture to Enhance GPT
T3.2	Manisha	Guduri	Generative Adversarial Networks for Active Implantable Medical Devices
T3.3	Shamik	Kundu	Towards Radiation-aware Functional Safety in Online AI Accelerators
T3.4	Alireza	Omidi	Transforming the Future of Brain Tumor Detection: A Hybrid Transformer-Based Approach
T3.5	Alireza	Omidi	A Transformer-Based Approach to Password Cracking in IoT Security Testing
T3.6	Alireza	Omidi	Cyber Fortification through Reconfigurable RO PUFs: Safeguarding IoT Devices Against Adversarial Intrusion, Reverse-Engineering, and Machine Learning Cyberattacks
T3.7	Pratik	Shrestha	ML-EDA Schema: A Graph Datamodel Schema and Open Dataset for Digital Design Automation
T3.8	Lorson	Blair	Low-bit quantization of Patch Time Series Transformer (PatchTST) Model
T3.9	Imane	Hamzaoui	Are Analog In-memory Computing the Future of Medical Imaging Segmentation?
T3.10	Shomoita	Mitin	Prediction of Gait Dysfunction in Patients with Parkinson's Disease from EEG signals