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CAS IEEE CIRCUITS AND SYSTEMS SOCIETY

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SBCCI is an international forum dedicated to integrated circuits and systems design, test and electronic design automation (EDA), held annually in Brazil. The 32nd SBCCI will take place in São Paulo, the largest city in Brazil. The goal of the symposium is to bring together researchers in the areas of EDA, design and test of integrated circuits and systems. The scope of the symposium includes technical sessions, tutorials and panels, as well as an exhibition and working group meetings. The best papers presented at the symposium will be invited to resubmit an extended version to be considered for publication at the IEEE Design & Test and at the Springer Nature ALOG (Analog Integrated Circuits and Signal Processing).

Location:

São Paulo is a cosmopolitan, melting pot city, also know as Sampa, is full of smart bistros and gourmet restaurants that make the city a world-renowned foodie haven. It is home to monuments, parks and museums such as the Latin American Memorial, the Ibirapuera Park, Museum of Ipiranga, São Paulo Museum of Art, and the Museum of the Portuguese Language.

Important Dates:

Abstract Submission:	March 20th, 2019
Paper Submission Deadline:	March 27th, 2019
Rebuttal period:	May 3rd-10th, 2019
Notification of Acceptance:	May 15th, 2019
Camera-Ready Deadline:	June 5th, 2019

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Paper Submission:

Prospective authors from around the world are invited to submit manuscripts in English for consideration by the Program Committee. Submissions of manuscripts previously published by other conferences or journals will not be considered by the program committee. SBCCI submissions must be made electronically (in PDF format) via the conference website. For proposals on special sessions, tutorials, panels and tool demos, please email a short description to the program chairs directly in advance of the submission deadline. The proceedings will be published by the IEEE XPLore and will be available at the ACM Digital Library and IEEE Xplore.

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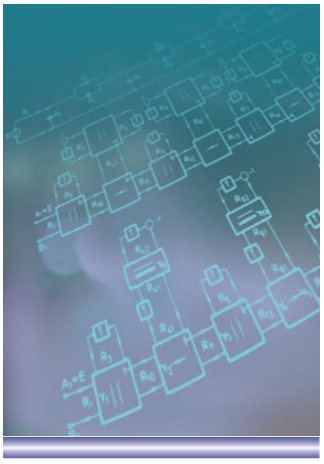
Features



ALFRED FETTWEIS

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Departments

Scope: Insofar as the technical articles presented in the proposed magazine, the plan is to cover the subject areas represented by the Society's transactions, including: analog, passive, switch capacitor, and digital filters; electronic circuits, networks, graph theory, and RF communication circuits; system theory; discrete, IC, and VLSI circuit design; multidimensional circuits and systems; large-scale systems and power networks; nonlinear circuits and systems, wavelets, filter banks, and applications; neural networks; and signal processing. Content will also cover the areas represented by the Society technical committees: analog signal processing, cellular neural networks, and array computing, circuits and systems for communications, computer-aided network design, digital signal processing, multimedia systems and applications, neural systems and applications, nonlinear circuits and systems, power systems and power electronics and circuits, sensors and micromaching, visual signal processing and communication, and VLSI systems and applications. Lastly, the magazine will cover the interests represented by the widespread conference activity of the IEEE Circuits and Systems Society. In addition to the technical articles, which may be seen as the centerpiece of the start-up plan, we plan also to cover Society administrative activities, as for instance the meetings of the Board of Governors, Society People, as for instance the stories of award winners-fellows, medalists, and so forth, and Places reached by the Society, including readable reports from the Society's conferences around the world.

Magazine Deadlines

Final materials for *IEEE Circuits and Systems Magazine* must be received by the Editor on the following dates:

Issue	Due Date
First Quarter	December 23
Second Quarter	April 1
Third Quarter	July 1
Fourth Quarter	September 15

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From the Editor

Chai Wah Wu
Editor-in-Chief, IEEE Circuits and Systems Magazine

Welcome to a new volume of the Circuits and Systems (CAS) Magazine! I want to wish everyone a happy 2019. One important event occurring this year is that the definition of the ampere will change, even though this will not have a significant impact to most of us in the CAS Society. More specifically, the new definitions of the fundamental units of kilogram, ampere, kelvin and mole which were agreed upon in November last year will come into effect on May 20. The ampere which used to be defined as the current needed to deposit silver at a certain rate via electroplating in a silver nitrate solution or to produce a specific force between two conductors, will now be defined as the flow of a fixed number of elementary charges per second. The kilogram has been defined as the mass of a platinum-iridium cylinder since 1889 and will be now defined in terms of the Planck constant. Similarly, the mole and the kelvin will be redefined using fixed constants. The prior definitions of these 4 fundamental units were all established in the 19th century and have served us well for over 100 years. Since this is the 19th volume of the magazine, I think it is appropriate to consider some of the other events in science and technology from the 19th century. In particular, I have been thinking about the interdisciplinary nature of circuits and systems and how practitioners in this field have influenced, learned from and collaborated with other scientific and technical communities.

Consider for example the impact of chemistry to circuits. It was exactly 150 years ago in 1869 that Mendeleev proposed his periodic table of the chemical elements [1]. This arrangement of elements by grouping them into metals, halogens, noble gases, carbon groups etc. help drive the development and understanding of semiconductors which eventually lead to modern electronic circuits. In the emerging area of quantum computing, metals such as vanadium, chromium, ruthenium are important elements in the construction of qubits [2].

It was also around this time that the chemical compound celluloid was patented [3]. This material was one of the first plastic compound that becomes pliable at high temperature and is widely used in photography and cinematography for many years and its pervasiveness in the motion picture industry led the term to be used to describe movies in general. About 50 years later a patent on another technology was filed: the Phonofilm technology [4]. This is one of the first sound-on-film technology where audio signals were encoded optically onto celluloid film for a synchronized audio track to the motion picture. Such chemical innovations go hand in hand with innovations in vacuum tube technology, audio and signal processing to accelerate the development of multimedia devices and platforms for our leisure and enjoyment.

Conversely, innovations in systems science has benefited the development of chemistry. During the same time when Phonofilm and related technologies were created, X-ray crystallography technology was being developed which combines imaging, tomography, and Fourier analysis to provide chemists an invaluable tool to determine and analyze the atomic structure of molecules [5]. More recently, quantum computers have been proposed to simulate the interaction of molecules and atoms [6].

I believe that the nature of the CAS society makes such cross fertilization natural. The concept of a system is technology agnostic. It can refer to a biological, chemical, social, electrical, mechanical or a physical system. For example, the concept of an arithmetic unit which forms the foundation of digital computers can be implemented in a variety of technologies, beginning arguably as mechanical gears in Babbage's Analytical Engine [7][1], which were superseded by electromechanical switches and purely electronic switches such as vacuum tubes and transistors. More recently, biological cells with programmable switching behavior have been realized [8]. Similarly, qubits in today's quantum computers can be realized in vastly different forms, such as photons, molecules, superconductors, etc. [9] and their quantum mechanical properties are described by the same mathematical equations.

Over the last few years I have looked for feature articles that celebrate this interdisciplinary nature to be

[1]Charles Babbage was a contemporary of Dmitri Mendeleev and unfortunately passed away before seeing a complete Analytical Engine being built. As of this writing there are plans to build a fully functioning Analytical Engine.

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President's Message

Yong Lian
President, IEEE Circuits and Systems Society (2018–2019)

Dear Members of the IEEE Circuits and Systems Society,

At the beginning of this New Year, I would like to convey my best wishes and sincere thanks to all of you. I wish you a very happy New Year full of happiness and success in your personal and professional lives. I would like to thank all volunteers for spending their time to serve the members and the Circuits and Systems (CAS) community. 2018 has been a very exciting year marked by many achievements and new initiatives for the society. We have many reasons to celebrate and look forward to another wonderful year ahead.

As I mentioned in the 2018 message, my goals as the President are to strengthen our technical leadership in the field of circuits and systems, and to create value for our members. What follows is a list of highlights of the many accomplishments we have achieved in 2018. I will group them into three areas: Technical Activities, Publications, and Member Services.

Technical Activities

The forthcoming wave of Artificial Intelligence (AI) could have a profound impact on all aspects of our society and lives. The society as the leader in the field of CAS has much to offer in AI ranging from AI hardware acceleration, energy efficient system architecture, design methodology and tools, emerging devices, to neuromorphic computing, algorithms, and applications. To facilitate the interaction among researchers, scientists, and engineers working in the field of AI, we will launch the first IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS) in March 2019 in Hsinchu, Taiwan. AICAS will serve as a platform for the society to promote AI related research and activities, and to provide trainings for those who want to work in AI. You are welcome to join this exciting event in March 2019. Thanks to Prof. Myung Hoon Sunwoo, VP Conferences, and AICAS Organizing Committee members for leading this effort.

While AICAS serves as a forum for disseminating knowledge and stimulating new ideas in AI, it is also important to reach out to the industry. For this purpose, we launched two very successful industry events, i.e. the First CAS-Silicon Valley AI for Industry Forum in Silicon Valley on September 21st, 2018 and the First IBM-CAS AI Compute Symposium at the IBM T.J. Watson Research Center THINKLab in Yorktown Heights, NY, on October 25th, 2018. Both events brought AI technology to the center of high-tech hubs. The Silicon Valley event was held in collaboration with Intel, where experts from Intel, Google, Facebook, and MIT covered a wide range of topics in AI from energy efficient system architecture, methods to accelerate deep neural networks, to centralized data processing. The event saw more than 330 attendees, of which 66% are non-IEEE Members. The presentation slides are available on the CAS Santa Clara Valley Chapter website: http://sites.ieee.org/scv-cas/2018/09/21/ieee-circuits-and-systems-society-silicon-valley-cas-sv-artificial-intelligent-for-industry-forum/. You are welcome to download these slides.

The IBM-CAS event was held in collaboration with IBM and the IEEE Electron Devices Society. The event had over 155 attendees from multiple companies and universities. It started with two keynote speakers from IBM and ARM, followed by two Invited Talks from Intel and IBM, and two Technical Sessions on "Bio-inspired Computing" and "Emerging Technologies". It also had a student poster session, where about 30 students presented their compelling research. The symposium closed with a panel discussion on "Artificial Intelligence or Artificial Stupidity: How smart will smart AI be?" The panelists included the keynote and invited speakers, as well as an IBM Fellow. The panel discussion will be available on IEEE TV. Feel free to watch this exciting event. In 2019, we plan to organize similar events around different parts of the world.

The successes of these events are not possible without our dedicated volunteers. I would like to thank Prof. Eduard Alarcon, VP Technical Activities, for investing his time into these wonderful events. I deeply appreciate Dr. Yen-Kuang Chen of Intel (a member of CASS BoG Technical Activities Division) for initiating the First CAS-Silicon Valley AI for Industry Forum, and Dr. Rajiv Joshi of IBM for organizing the First IBM-CAS AI Compute Symposium.

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Brain related electronics is another field that CASS is deeply involved in. In 2016, the society launched the first Brain Circuits and Systems workshop (BrainCAS) as a side event of BioCAS2016. BrainCAS is dedicated to promote collaborations between very different disciplines. In 2018, we initiated a NeuroCAS Workshop as a post BioCAS2018 event, which focuses on ECoG and peripheral/autonomic nervous system interfaces and prostheses. A mixture of structured discussions and informal networking sessions encouraged researchers, scientists, and clinicians to generate novel research ideas and build new collaborations. Thanks to Prof. Tim Constandinou (a member of CASS BoG Conference Division) and the team for the great job!

Food is important to everyone. In 2017, we launched the Food Circuits and Systems Workshop (FoodCAS) along with BioCAS2017. This year for the first time, FoodCAS will become a satellite event of ISCAS2019 in Sapporo, Japan. It will focus on a wide range of technologies that CASS can offer to smart agriculture. More details can be found at: http://www.knt.co.jp/ec/2019/foodcas/. Thanks to Prof. Danilo Demarchi and the team for organizing the first FoodCAS satellite workshop in ISCAS2019.

In addition to the aforementioned events, we also organized a UK CAS Tutorial on Biomedical Circuits and Systems, three Seasonal Schools on Physical Design Automation, Logic Synthesis and Verification, Industry Internet-of-Things, respectively. Similar events will be organized in 2019. We welcome you to send us your proposal if you are interested in organizing a Seasonal School in your region or country in 2019.

Publications

Publications are an important platform for the society to disseminate knowledge to the readers. The quality of CAS publication reflects our technical strength in the field. I am glad to report that under the leadership of Prof. Manuel Delgado Restituto, VP Publications, and the effort from the Editor-in-Chiefs, Editorial Boards, Reviewers, and authors, almost all CASS journals are achieving their best performance, including the Impact Factor, Eigenfactor Score, and Article Influence Score. Congratulations to our Editor-in-Chiefs, Dr. Andreas Demosthenous of TCAS-I, Dr. Chi K. Michael Tse of TCAS-II, Dr. Shipeng Li of TCSVT, Dr. Mohamad Sawan of TBioCAS, and Dr. Eduard Alarcon of JETCAS.

Fast publication is one of our goals for CAS journals. This year, we invested heavily to increase the number of pages for our main publications including IEEE Transactions on Circuits and Systems I (TCAS-I), IEEE Transactions on Circuits and Systems II (TCAS-II), IEEE Transactions on Circuits and Systems for Video Technology (TCSVT), IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), and IEEE Journal on Emerging and Selected Topics on Circuits and Systems (JETCAS). We have allocated more than 2800 extra pages for the above journals to shorten the time from e-publication to printed version. This is the largest increase in page budget for CAS journals in the recent years. Our target is for all our journals to go from e-publication to printed version in less than 6 months.

Circuits and systems are in the frontier of many emerging fields. To meet the demand of authors and readers, we created a new platform in 2018, i.e. a journal tracked conference called "International Symposium on Integrated Circuits and Systems" (ISICAS). It is established to attract high quality papers while providing opportunities for authors to share their results with the public in a very short time frame. ISICAS is a new form of conference, where all accepted papers are published in the Special Issues of TCAS-I and TCAS-II in 2018. Authors are given the opportunity to present their results to a large group of audience during the conference. The paper processing time is extremely fast, i.e. less than 6 months from paper submission to publication, which sets a record in any CAS sponsored journals. The success of ISICAS2018 inspired us to offer more to our members and authors. In 2019, in addition to TCAS-I and TCAS-II, TBioCAS will join the ISICAS2019. Authors can submit their papers to the ISICAS2019 Special Issues of TCAS-I, TCAS-II, and TBioCAS before March 1st, 2019. ISICAS2019 will be held in Venice, Italy from August 29-30, 2019. Details can be found at http://ims.unipv.it/ISICAS19/. Thanks Prof. Franco Maloberti, Past President, and the ISICAS2019 team for this great initiative.

Member Services

As a professional society, members are the most important assets to the society. At the management level, we are committed to improving services, creating values, reaching out to the industry and YPs, and promoting Women in Engineering. Chapters are the focal points for serving our members in different regions. In 2018, we initiated the following outreach programs at the local level:

- Low Power Image Recognition Challenge
- CASS Spinoff Ideas Contest
- Industry outreach programs: (1) CAS-Silicon Valley AI for Industry Forum, and (2) IBM-CAS AI Compute Symposium
- Outreach for Student Branch Chapters
- African Workshop on Circuits and Systems
- South-East Asia Workshop on Circuits and Systems
- CAS Workshops in South China
- Local workshops for newly formed chapters
- Region 1-7 Student Research Competition
- Region 8 Chapters Workshop Tour

- Region 9 Industry Tour
- Region 10 Networking CASS Chapters

The feedbacks we have gotten from the above programs are very positive. We are going to invest more in chapters to boost local activities in 2019. I am happy to report that the society registered a healthy increase in its membership in 2018, i.e. 5.24% increase in overall membership, and 16.15% increase in Region 10. In addition, 4 new CAS Chapters and 6 new Student Branch Chapters were created in 2018. Thanks to Prof. Yoshifumi Nishio, VP Regional Activities & Membership, for being very active in organizing events and recruiting members.

Most IEEE journals set a "page break" on how many free pages the author(s) can have for their paper. For CAS publications such as TCAS-I, TCSVT, TBioCAS and JETCAS, the "page breaks" are 9 pages, i.e. every paper can have up to 9 free pages. After the "page break" of 9 pages, each additional page was charged at an over-length page charge of $175 per page. This over-length page charge can create a financial burden to many authors. In order to help our authors, the society has invested the operational surplus to reduce the over-length page charge from $175 to $125 per page. Furthermore, the "page breaks" for TCAS-I, TCSVT, TBioCAS and JETCAS have increased from 9 to 11 pages in 2018, i.e. the authors will have 11 free pages for each accepted paper. We hope that the increase in "page break" and the decrease in over-length page charge will encourage authors to publish papers in CAS journals. The society will continue this practice if the operational surplus is sufficient to support it.

The review process of CAS journals relies on the EDICS (Editor's Information Classification Scheme), which is used to help the Editor-in-Chief to select the best reviewers for a submitted paper. With the fast change in the CAS field, it is necessary to keep the EDICS up to date. Under the leadership of Prof. Eduard Alarcon (VP Technical Activities) and Prof. Manuel Delgado Restituto (VP Publications) and with the help of all Editors and Technical Committees, the existing EDICS has been reviewed and revised to clearly define the fields of interests of CAS journals. We will update the EDICS in 2019. We hope the new EDICS will help authors to better classify their papers and speed up the review process.

Continuous education is an important part of life long learning. To provide more educational resources to our members, we published four e-books in 2018,

- "Power Management for Internet of Everything" edited by Sergio Saponara (University of Pisa, Italy)
- "Enabling Technologies for the Internet of Things: Wireless Circuits, Systems, and Networks" edited by Mathieu Coustans and Catherine Dehollain (both of EPFL, Switzerland)
- "Low Power Circuit Design Using Advanced CMOS Technology" edited by Milin Zhang and Zhihua Wang (both of Tsinghua University, China), Jan Van der Spiegel (University of Pennsylvania, USA) and Franco Maloberti (University of Pavia, Italy)
- "Circuits and Systems for Biomedical Applications – UKCAS2018" edited by Hadi Heidari (University of Glasgow, UK) and Sara Ghoreishizadeh (University College London, UK).

These books are free for CAS members. You can download them from the CAS Resource Center at: https://resourcecenter.cas.ieee.org/.

WiCAS (Women in Circuits and Systems) and YPs (Young Professionals) are two focus groups within CASS. WiCAS group promotes CAS activities among women engineers and researchers, while YP group helps the society to design programs suitable for young professionals. We have a dedicated WiCAS event in ISCAS every year. I welcome you to attend the WiCAS session in ISCAS2019 in Sapporo, Japan. In 2018, we also launched the YP Mentoring Sessions in CAS flagship conferences, including ISCAS2018, APCCAS2018, and ICECS2018. These mentoring sessions serve the following purposes: (1) to introduce YPs to the world of CASS; (2) to facilitate experience sharing amount members; (3) to provide advice in early career development; (4) to encourage YPs to actively participate in CAS related activities; (5) to create opportunities for YPs to volunteer their services to the society; and (6) to attract YPs to join the society. The YP sessions will be organized regularly in our flagship conferences. We encourage YP members to participate in these sessions in 2019. Thanks Prof. Jennifer Blain Christen for leading the effort for WiCAS group and Prof. Hadi Heidari for YP Group.

I am deeply grateful to all volunteers for their hard work and commitment to serve the society, which have made these accomplishments possible. Thanks to Prof. Franco Maloberti (Past President) for leading the Nominations, Constitution and Bylaws, and Awards committees, Dr. Amara Amara (President-Elect) for chairing the Long Term Strategy Committee, Prof. Chang Wen Chen (VP Financial Activities) for managing the finance of the society. Thanks to Prof. Pamela Abshire, Prof. Elena Blokhina, Dr. Gabriele Manganaro, Prof. Mohamad Sawan, and Prof. An-Yeu (Andy) Wu for serving the Board of Governors (BoG) in the past three years. Special thanks to the following members, who chair the various committees in the society:

- Prof. Enrico Macii, Chair of Society Fellow Evaluation Committee.
- Prof. Joos Vandewalle, Chair of Charles A. Desoer Technical Achievement Award Subcommittee.

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From the Guest Editors

Sankar Basu
National Science Foundation

Patrick Dewilde
Technical University of Delft

This issue of the CAS magazine presents papers that could not be accommodated in the 1st part of the Alfred Fettweis memorial special issue that appeared as the December 2018 issue. While the 1st part provided extensive views of Alfred Fettweis' personal life, scientific contributions, and several papers dealing with areas that were influenced by his scientific and technological contributions at large, many other topics could not be included due to multiple reasons which included primarily lack of space, and also the vast expanse of diverse topics that Fettweis had worked on during his long career – both before and after his formal retirement from the scientific/technical enterprise.

On a more informal note, it may be relevant to mention here that the IEEE Circuits and Systems Society, led by its two past presidents Josef Nossek and Hari Reddy, had organized a memorial special session at the 2016 International Symposium on Circuits and Systems (ISCAS) held in Montreal, where the idea of a special issue was conceived. While several of the contributors to the part-1 and part-2 of the present special issue of the CAS magazine spoke at that session, all participants of the ISCAS 2016 special session had, at least in principle, agreed to contribute to a special issue of this type. Meanwhile, some of the articles promised at the ISCAS 2016 special session were not received in the end due to various reasons, including personal situation of the authors or timeliness of a submission appropriate for the special issue. A copy of the program, and a collage of pictures from the ISCAS 2016 special session and other events spanning Alfred Fettweis' life will be available in an upcoming issue of the IEEE CAS Newsletter.

This 2nd part essentially contains three technical papers relevant to Alfred Fettweis' contributions. All of them were originally slated for part-1, but due to restrictions on the number of pages allowed in an issue, they had to be moved to part-2. While the EiC of the CAS magazine was kind enough to allow a part-2 to accommodate lengthy papers, the choice to move these papers to part-2 was taken collectively by the EiC and the guest editors of this special issue.

The first such paper "Robust digital filter structures: a direct approach" by P. P. Vaidyanathan and Sanjit K. Mitra deals with alternate methods of deriving structurally passive digital filters directly in the digital domain that were inspired by the wave digital filters of Alfred Fettweis and had to be originally derived from continuous domain prototypes (orthogonal filters are other examples of this type). It is well known that Sanjit Mitra had been an old friend and professional colleague of Alfred Fettweis going back about 40 years, and P. P. Vaidyanathan had completed his PhD dissertation under Prof. Mitra on precisely the same topic at the University of California at Santa Barbara in the early 1980s.

The 2nd paper "Symmetry Incorporated Cost-Effective Architectures for Two-Dimensional Digital Filters" by Lan-Da Van, I-Hung Khoo, Pei-Yu Chen, and Haranatha (Hari) C. Reddy deals with VLSI implementable 2-D filter architectures incorporating different symmetries. Two-Dimensional Digital Filters had been one of Alfred Fettweis' research interests. Hari Reddy recollects that he first met Professor Fettweis in 1973 at Osmania University in Hyderabad, India, while he was working towards his Ph.D. Degree. Professor Fettweis then served as an external examiner of his Ph.D. dissertation. Since that time, Hari and Professor Fettweis interacted closely for four decades on research, CAS society administrative matters, and more importantly on personal welfare issues for which Hari has been very grateful.

The third paper of this issue on "Nonlinear circuit simulation by Alfred Fettweis' wave digital principles" is by Tim Schwerdtfeger and Anton Kummert. Anton Kummert was one of the prominent students of Alfred Fettweis who completed both his doctoral dissertation and Habilitation in Alfred's group in Bochum in the late 1980s. While the Wave Digital filters were originally proposed and used in industry for frequency filtering only, the paper attempts to establish use of the basic wave digital techniques in SPICE-like circuit simulation applications.

The abovementioned papers, including those published in part -1 of this memorial special issue, are only

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a sampling of the wide variety of topics that Alfred Fettweis worked on. Many of the other topics of interest to him remain unaddressed in this two-part special issue. Such topics, among others, include switched capacitor filters, broad band matching problems, and his foray into problems of foundational physics. We encourage readers to further explore both the topics covered in the two issues and those not presented. They all contain vectors to further research and potential new discoveries.

From the Editor *(continued from page 3)*

published in the magazine and I encourage all prospective authors to view the magazine as a venue for manuscripts not necessary limited to traditional CAS topics.

In this first issue of the year, we collected several invited papers dedicated to the memory of Prof. Alfred Fettweis that could not be accommodated in the last issue due to space limitations and late submission. For the rest of the year, we have planned some exciting feature articles and special issues and we hope that they provide further ideas of fruitful collaboration with other disciplines.

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President's Message *(continued from page 6)*

- Prof. Randall Geiger, Chair of Society Education Award Subcommittee.
- Dr. Gabriele Manganaro, Chair of Industrial Pioneer Award Subcommittee.
- Prof. Tor Sverre Lande, Chair of Mac Van Valkenburg Award Subcommittee.
- Prof. Wouter Serdijn, Chair of Meritorious Service Award Subcommittee.
- Prof. Yoshifumi Nishio, Chair of Chapter-of-the-Year Award Subcommittee, Chair of Student Travel Awards subcommittee, Chair of Pre-Doctoral Scholarship Subcommittee.
- Prof. Manuel Delgado Restituto, Chair of Biomedical Circuits and Systems Best Paper Award Subcommittee, Chair of Circuits and Systems for Video Technology Best Paper Award Subcommittee, Chair of Darlington and Guillemin-Cauer Best Paper Awards Subcommittee, Chair of Outstanding Young Author Best Paper Award Subcommittee, Chair of Very Large Scale Integration Systems Best Paper Award Subcommittee.
- Prof. Elvis Mak, Chair of Distinguished Lecturer Selection Committee.

In 2019, we will maintain our momentum and continue to work hard to achieve our goals, i.e. to strengthen our technical leadership in the field of circuits and systems, and to create value for our members. I invite you to join us to make CASS a better home for all our members. I thank you once again for what you have done, and what great things I anticipate that you will do for the society in 2019.

Recognitions

New IEEE Fellows

Members of CASS and Evaluated by CASS

Jill M. Boyce, *for contributions to video coding*

Luca Fanucci, *for the contributions to the design of Very-large-scale integration systems for network-on-chip*

Maysam Ghovanloo, *for contributions to implantable wireless integrated circuits and systems*

Chris Hyung-il Kim, *for contributions to on-chip circuit reliability evaluation and characterization*

Pui-in Mak, *for contributions to radio-frequency and analog circuits*

Yap-peng Tan, *for contributions to visual data analysis and processing*

Shaojun Wei, *for leadership in integrated circuits engineering of smart cards and reconfigurable devices*

Xiaokang Yang, *for contributions to perceptual modeling and processing of visual signals*

Weisheng Zhao, *for contributions to spintronic integrated circuit design*

Members of CASS and Evaluated by Other IEEE Entities

Meng-fan Chang, *for contributions to static and nonvolatile memories for embedded systems*

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Deming Chen, *for contributions to FPGA high-level synthesis*

Antun Domic, *for technical leadership in the integrated circuits design automation*

Christian Enz, *for contributions to low-power analog circuit design*

Joseph Evans, *for contributions to cognitive networks and deployment of defense networks*

Hossein Hashemi, *for development of radio-frequency and optical phased-array integrated circuits*

Gang Hua, *for contributions to facial recognition in images and videos*

Tao Jiang, *for contributions to coding, modulation, and cognitive radio systems design*

Farinaz Koushanfar, *for contributions to hardware and embedded systems security and to privacy-preserving computing*

Hai Li, *for contributions to neuromorphic computing systems*

Tao Mei, *for contributions to multimedia analysis and applications*

Maurizio Porfiri, *for contributions to biomimetic robotics*

Seishi Takamura, *for application of video coding*

Hiroto Yasuura, *for contributions to energy-efficiency and dependability of Very Large Scale Integration designs*

CAS Society News

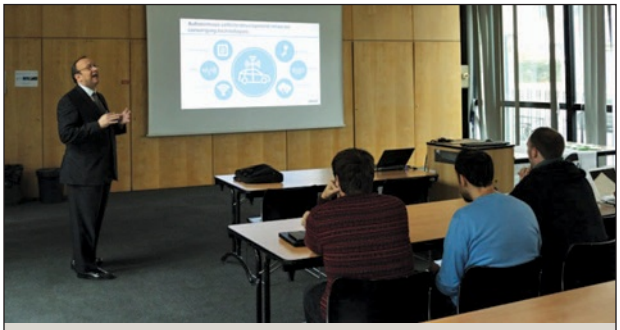
IEEE CAS Distinguished Lecture

IEEE CAS Society France Section invited Prof. Ashraf Salem, Engineering Director in Mentor A Siemens Business to deliver an IEEE CAS Distinguished Lecture on October 2, 2018. The lecture was held at Telecom ParisTech, Paris, France

In his lecture, "Automotive Digital Twin: ADAS System verification", Prof. Salem discussed how Automotive OEMs will take more control of Electronic Control Unit (ECU) hardware/software architecture definition and exploration. This is due to the rise of new technologies in ADAS and autonomous vehicles. He explained that the increasing number of cars with ECUs containing tens of processors, and the need to accelerate the simulation of thousands of driving scenarios and design parameters to ensure safety and reliability in autonomous driving has expanded the use of hardware emulation in the loop based on its capacity and functional verification merits.

In his presentation, he showed an integrated heterogeneous system of systems framework to simulate and verify multiple ECUs. The framework includes ADAS scenarios simulator, mechanical simulator, virtual platforms and RTL Designs. The distinguished lecture attracted more than 15 faculty members and graduate students in Telecom ParisTech. There were many questions and fruitful discussions with the audience.

Before and after his lecture, Prof. Salem visited Telecom ParisTech and discussed with researchers from the laboratory about information processing and communication (LTCI).



Prof. Ashraf Salem presents his topics.

Santa Clara Chapter

The IEEE CAS Society (CASS) Santa Clara Chapter (SCV) co-sponsored an event with Solid-State Circuits Society (SSCS) and Signal Processing Society (SPS) that was held on July 19th, 2018 at TI Auditorium in Santa Clara, CA. The lecture titled "Review of Lidar, Localization and Object Processing for Safe Autonomous Systems" was given by Dr. Kiran Gunnam. In the first part of his talk, Dr. Gunnam reviewed the state-of-the art architectures for LiDARs, lasers, photo diodes, transmitters and receivers including time to digital conversion, matched filtering for detection and cross-talk avoidance. In the second part of the talk, he described recent groundbreaking work (by Apollo AI) in integrated perception that can be easily embedded into the LiDAR sensors which consists of LiDAR+camera+IMU fusion, robust mapping, localization and object processing for safe autonomous systems. The total attendance for this event was 118.

The "Artificial Intelligence for Industry Forum," sponsored by Circuits and Systems Society, was held on September 21st, 2018 at Intel Auditorium in Santa Clara, CA. The event was organized by Dr. Yen-Kuang Chen and Dr. Tong Zhang at Intel Corporation and co-sponsored by Santa Clara chapters of CAS, SSCS, ComSoc, SPS, and CIS. The speakers invited to this forum were: Dr. Debbie Marr (Intel), Dr. Vivienne Sze (MIT), Dr. Mark Sandler

Prof. Ashraf Salem with lecture attendees.

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(Google), and Dr. Jongsoo Park (Facebook). The event attracted 334 attendees that included IC designers, systems and software engineers, academics, and students from local industry and schools.

On October 18th 2018, CASS co-sponsored an lecture event with SSCS and Computer Society (CS) titled, "Efficient Circuits and Systems for Computational Imaging and Vision on Mobile Device," which was given by Dr. Prianka Raina. Dr. Raina began her talk by motivating the audience on the need for energy-efficient hardware accelerators targeted for image processing on mobile devices. The images taken on a mobile device involve a number of computational imaging algorithms such as high dynamic range (HDR) imaging, panorama stitching, image deblurring and low-light imaging. Because of their high computational complexity, mobile CPU or GPU based implementations of these algorithms do not achieve real-time performance. Moreover, offloading these algorithms to the cloud is not a viable solution because wirelessly transmitting large amounts of image data results in long latency and high energy consumption, making them unsuitable for mobile devices. Dr. Raina's approach to solving this problem has been to design energy-efficient hardware accelerators for these applications. She described the implementation of three complete computational imaging systems for energy-constrained mobile environments, energy minimization techniques, and energy scalability by trading off accuracy with execution time. The total attendance for this event was 70.

Next joint event between SSCS and CASS was held on November 15th, 2018 where Dr. Laurence Nagel gave an interesting talk on "The Life of SPICE." Dr. Nagel gave a historical account of the most popular circuit simulation program in the world. What began as a teaching program at the University of California, Berkeley, spread into industry and has been around for almost fifty years! The total attendance for this event was 68.

On December 6th, 2018 CASS organized a lecture given by Dr. Hans Klein who is currently the Analog CTO at Cypress Semiconductor Corp. The lecture titled "Advanced Capacitive Sensing for Consumer, Industrial, and Automotive Applications," was given at the Main Auditorium at Cypress Semiconductor Corp. San Jose Campus. The lecture covered basic and advanced capacitive sensing for a variety of consumer, industrial, and automotive applications such as "single-pixel" buttons, sliders, touch screens, and "kilo-pixel" fingerprint readers. In addition, sensors, architectures, algorithms, and circuit technologies to handle signals from the pF range all the way to fractions of an aF were discussed. The last part of the lecture described future challenges and emerging solutions. The event attracted 42 attendees that included IC designers, academics, and students from local industry and schools and another 8 joined remotely on Zoom conference system.

Future Events: We have 4 talks confirmed in 2019 and two of those are CASS Distinguished Lecturer Events. The first lecture will be held on Jan 31st, 2019 in the Main Auditorium at Cypress Semiconductor Corp. San Jose Campus. That lecture is on "Vehicle Re-Identification for Smart Cities: A New Baseline Using Triplet Embedding" and will be given by Dr. Ratnesh Kumar who is currently working in Deep Learning for Computer Vision at nVidia Inc. The second lecture is tentatively planned on February 22nd, 2019 and will be given by Dr. Massimo Alioto who is part of the Green IC group at National University of Singapore. While the agenda for the lecture is not finalized, we expect it will include topics such as Hardware Security, Energy-autonomous Systems and Wireless Sensors. The last two talks are CASS Distinguished Lecturer events. The lecture on March 8th, 2019 given by Dr. Gabriel A. Rincón-Mora from Georgia Tech will cover topics such as Energy-Harvesting, Piezoelectric Chargers, Photovoltaic Charger, and Inductively Powered Battery Chargers. The lecture on April 25th, 2019 given by Dr. Alyssa Apsel from Cornell University will cover topics such as Ultra Low Power Radios, Flexible Radios and Flexible Networks. We plan on broadcasting these events live using Zoom conference system.

The recordings of our past events with Dr. Gabor Temes and Dr. Mihai Banu are now on IEEE TV (https://ieeetv.ieee.org) and have been viewed 139 and 239 times respectively. The recent lecture on Capacitive Sensing by Dr. Hans Klein will be posted on IEEE TV soon. You can join our events from any-where around the world through Zoom. Sign up for our listserv (http://sites.ieee.org/scv-cas) to get event notification and registration

CASS AI Forum speakers, organizers, sponsors, and co-sponsoring society officers. From left to right: Dr. Yen-Kuang Chen (CAS Board of Governors/Intel), Dr. Tong Zhang (Intel), Robert S. Ogg (CAS-SCV Chair), Dr. Yong Lian (CAS President), Dr. Jongsoo Park (Facebook), Dr. Mark Sandler (Google), Dr. Vivienne Sze (MIT), Dr. Debbie Marr (Intel Labs), Eduard Alarcón (Vice President - Technical Activities CAS), Mojtaba Sharifzadeh (SSCS-SCV Chair), and Dr. Mehran Nekuii (ComSoC-SCV Vice-Chair).

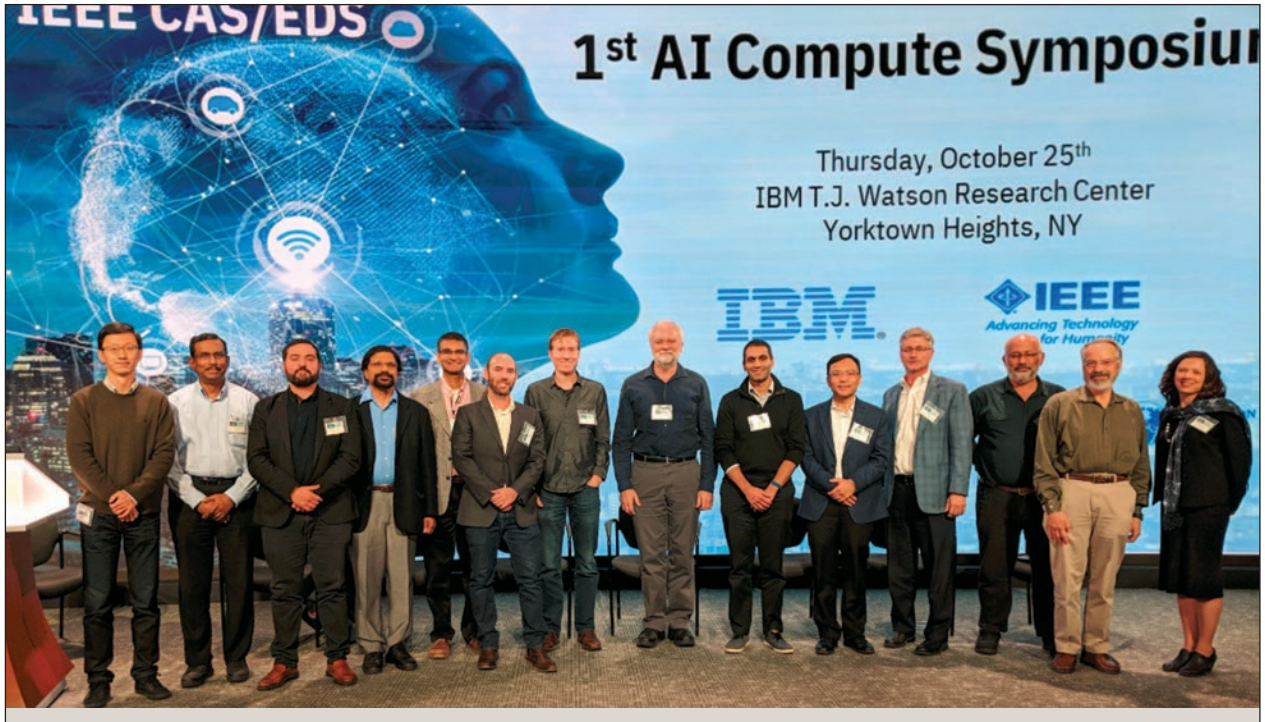
information. Only those who register for the event will be sent Zoom Conference details one day before the event. Also, please visit our Facebook website (by typing "IEEE SCV CAS" string) for event details and pictures.

1st AI Compute Symposium

Together with the IEEE CAS Society and the IEEE Electron Device Society (EDS), IBM Research led the 1st AI Compute Symposium at the IBM T.J. Watson Research Center THINKLab in Yorktown Heights, NY, on October 25th 2018. This symposium brought together dreamers, thinkers, and innovators across industry and academia together for a one-day symposium focusing on cutting-edge research addressing AI Compute challenges and future directions of AI. The symposium consisted of two keynotes, six invited talks, a student poster session, and a panel discussion. The event was free of charge and had over 155 attendees from IBM, various companies and universities. IBM along with IEEE indeed showcased leadership and advancement in AI-Compute domain.

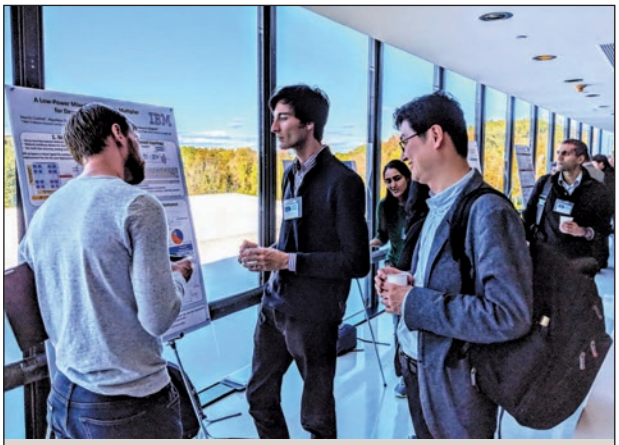
Keynote talks were delivered by Lisa Amini from IBM and Rob Aitken from ARM. Lisa Amini provided an inspiring overview of research projects from the MIT-IBM Watson AI Lab, which has recently celebrated a one-year anniversary. Amini described three tiers of AI research spanning narrow, broad, and general AI. She posited that the AI research community is beginning a journey into broad AI, whereas general AI is still a long-term goal for the future. Rob Aitken followed with a keynote address describing how many emerging AI problems present dynamically changing goals and rules, rather than the fixed goals and rules of conventional computing problems. Aitken also presented practical approaches for decomposing complex problems into manageable components that may provide a path for tackling complex AI challenges. Finally he concluded that the IoT needs distributed systems with AI. ML application to IoT involves real time application, explainability and security.

Following the keynotes, Mike Davies from Intel and Jeff Burns from IBM gave invited talks during the "Industry Perspectives" session. These talks provided a landscape of industrial research for both near and long term, spanning architectural, circuit design, and semiconductor technology. Mike Davies' talk focused on Intel's Loihi neuromorphic chip as well as future directions in neuromorphic research. Although Loihi is a digital chip, this avenue of research pushes beyond conventional von-Neumann architectures. On the other hand, Jeff Burns' talk focused on current efforts and future plans for deep learning acceleration.



Committee and Invited Speakers, L to R: Xin Zhang (IBM), Krishnan Kailas (IBM), Eduard Alarcon (UPC Barcelona Tech), Rajiv Joshi (IBM), Arvind Kumar (IBM), Matt Ziegler (IBM), Mike Davies (Intel), Rob Aitken (AMD), Naveen Verma (Princeton University), Wei Lu (University of Michigan, Ann Arbor), Todd Hylton (UC San Diego), Andreas Andreou (John Hopkins), Mark Wegman (IBM), and Pamela Abshire (University of Maryland).

Poster winner.



Poster session.

Burns described a vision beginning with specialized digital accelerators in the near term with enhancements based on analog circuit design and future device technology in the future.

Next, in the "Bio-inspired Computing" session, Andreas Andreou from Johns Hopkins University provided a number of examples of bio-inspired chip designs, many of which are components in systems that solve complex problems of interest to organizations like DARPA. In arguably the most provocative talk of the day, Todd Hylton from the University of California, San Diego, proposed the concept of thermodynamic computing as a potential future direction for computing research. Its evolution can be biased through programming, training and rewarding.

The third session on "Emerging Technologies" included talks by Wei Lu from the University of Michigan and Naveen Verma from Princeton University. Lu described recent research progress on RRAM (resistive random access memory) device and chip-level design and fabrication. He described how RRAM can provide a platform for neuromorphic computing, which is a promising direction for future AI computing. Naveen Verma delivered a case for circuit and architectural approaches for in-memory computing, another topic of high interest to the community. He presented measurement results from several fabricated chips providing compelling evidence for in-memory computing potential.

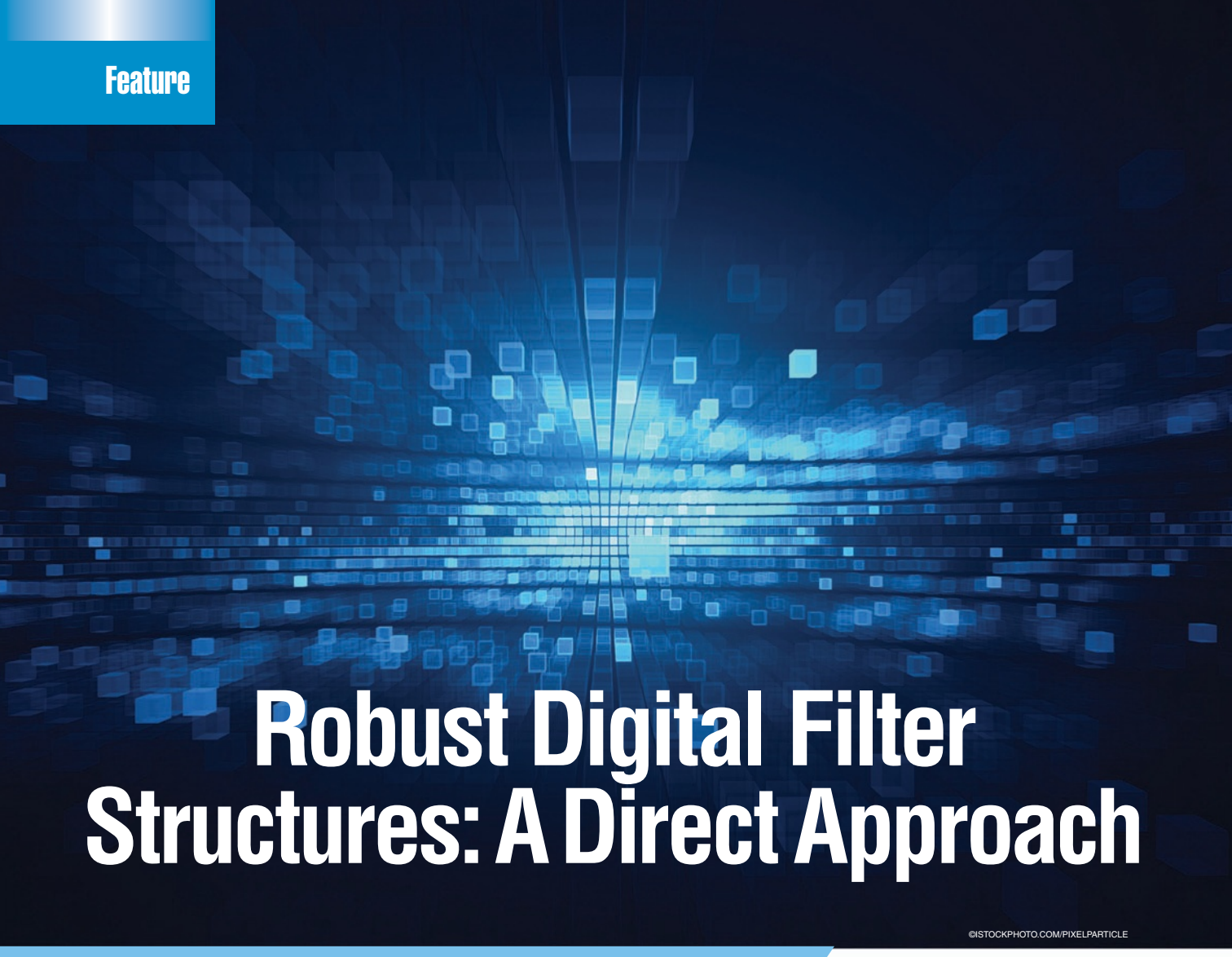
The symposium also had a well-attended student poster session, where about 30 students presented compelling research spanning numerous topics in AI computing. Two best poster presentations were awarded. One award was given to Sohum Datta from UC Berkeley for work on "A 2048-dim General-purpose Hyper-Dimensional Processor." A second award was given to Jingcheng Wang from the University of Michigan for "Neural Cache: Bit-Serial In-Cache Acceleration of Deep Neural Networks."

The symposium closed with a panel discussion entitled "Artificial Intelligence or Artificial Stupidity: How smart will smart AI be?" The panelists included the keynote and invited speakers, as well as IBM Fellow Mark Wegman. A lively and at times heated debate ensued where topics from the progress in AI research to AI ethics were touched upon. Todd Hylton presented a case that while progress in narrow AI challenges have made progress, the community is far from approaching true intelligence. At times Andreas Andreou and Mark Wegman sparred over the future of AI research progress, while Naveen Verma wound up as the mediating voice. The panel discussion is scheduled to appear IEEE TV in the near future.

Overall, the general consensus of attendees, speakers, and organizers was that day provided a great platform for educational forum and lively discussions related to the most current compelling topics in the computing field. Additional publications (Book, Journal papers etc) based on the symposium technical content are planned to provide educational resources for anyone interested. Although early in the stages, future events based on AI Compute are being planned by IBM and IEEE, please see the following website for updates: http://ibm.biz/AIcomputesymposium

Last year IBM, CAS and EDS sponsored first of a kind emerging technology symposium (focusing on Neuromorphic, Quantum, Security based computing). It was attended over 180 folks and was major success in educating and directing the audience in the emerging directions. This initiative by CAS to attract industry folks is really paying off. Also it is driving the technology landscape with the help of industry. A true symbiotic process.

Many thanks to Patricia Desgreys, Imran Bashir, Brittian Parkinson, Rajiv Joshi, Matt Ziegler, Arvind Kumar, and Eduard Alarcon who contributed to this report.



Robust Digital Filter Structures: A Direct Approach

P. P. Vaidyanathan, Fellow, IEEE and Sanjit K. Mitra, Life Fellow, IEEE

Abstract

One of the many contributions of Prof. Fettweis was the invention of wave digital filters. These filters are obtained from classical RLC filters, in particular doubly terminated lossless two-ports, by using some transformations. Namely, the voltages and currents in the circuit elements are transformed into wave-variables and then a bilinear transformation is performed. If the wave transformation is performed appropriately it results in a realizable digital filter structure which furthermore enjoys a number of robustness properties such as low passband sensitivity, low roundoff noise, and freedom from limit cycle oscillations. Prof. Fettweis and his colleagues also showed that these properties are due to the inheritence of passivity properties from the continuous-time domain into the digital filter domain. Subsequent to this landmark work, a number of researchers worked on the problem of obtaining robust digital filter structures without starting from continuous-time circuits. One of these is the structurally bounded or structurally passive class of digital filters. These structures are based on inducing structural passivity directly into the implementation and are therefore simpler, both conceptually and from a practical viewpoint. They are also more general and lead to new structures which have no natural connection to electrical circuits. This paper gives an overview of some of these developments.

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I. Introduction

Prof. Fettweis was a giant in many different areas of circuit theory, signal processing, physics and related mathematics. One of his contributions was the invention in 1971 of wave digital filters [18], [19]. These filters are obtained from classical *RLC* filters [35], in particular doubly terminated lossless two-ports, by using some transformations. Namely, the voltages V_i and currents I_i in the circuit elements are transformed into wave-variables using formulas of the form

$$A_i = V_i + R_i I_i \quad B_i = V_i - R_i I_i \tag{1}$$

where A_i and B_i are called the "incident" and "reflected" wave variables, and $R_i > 0$ are free parameters to be chosen by the designer. In addition to *RLC* elements, transformers and gyrators are also sometimes included. If the wave transformation is performed appropriately, then the bilinearly transformed version of the circuit results in a realizable digital filter structure (i.e., a structure without delay-free loops), which furthermore enjoys a number of robustness properties such as low passband sensitivity, low roundoff noise, and freedom from limit cycle oscillations [26]. Prof. Fettweis and his colleagues also showed that these properties are related to the passivity properties of the underlying continuous time electrical circuit [20].

Subsequent to this landmark work, a number of researchers explored the possibility of obtaining robust digital filter structures without starting from continuous-time circuits. This includes the work of Bruton and Vaughan-Pope [10], Constantinides [13], Mitra and Sherwood [49], Deprettere and Dewilde [15], Rao and Kailath [59], and Vaidyanathan and Mitra [71], [74], [77]. Some (but not all) of these structures exhibited low sensitivity and other robustness properties. These include the structurally bounded class of digital filters [71], [73], [77], and orthogonal digital filter structures [15], [59].

The structurally bounded or structurally passive class of digital filters [71] are based on inducing passivity directly into the structure and are therefore simpler, both conceptually and implementation wise. They explain in a unified way the robustness properties of wave digital filters, wave lattice filters [21], orgthogonal digital filters [15], [59], and the Gray-Markel lattice structures [32]–[34]. The structurally bounded class is also more general and leads to new structures which have no natural connection to electrical circuits such as the cascaded FIR power complementary lattice [78], the FIRBR structure [74], and the single-input two-output IIR power complementary lattice [59].

This paper gives an overview of some of these developments. We first review the fundamental reason for the low sensitivity of doubly terminated lossless networks based on an argument advanced by Orchard in 1966 [55], [56]. After a brief review of wave digital filters we explain structural boundedness in detail. The approach of structural boundedness [71] is based on the premise that if boundedness can be directly realized in the digital domain by constraining the structure, then there is no need to copy electrical circuits into the digital domain using painstaking and detailed formulas. We also discuss a number of robust digital filter structures derived using structural boundedness. It turns out that the two-port extraction method proposed by Mitra, Kamat, and Huey [50] long before the introduction of structural boundedness, can in fact be used to develop cascaded networks with structurally bounded properties. The beauty is that this procedure gives rise to wave filters, Gray-Markel lattices, and orthogonal digital filters as special cases [75]. But that is not all. Many new low sensitivity structures, not based on the two-port cascade, emerge from the theory of structural boundedness. Some of these are reviewed here as well, such as the parallel allpass structure [77], FIR power complementary lattices [78], and FIRBR structures [74].

II. Low Sensitivity and Structural Boundedness

When a digital filter is implemented with finite precision for the multiplier coefficients, the response $H(e^{j\omega})$ changes, and may fail to satisfy the original specifications. In fact the filter may even become unstable if the number of bits used for the multipliers is too small. Figure 1 shows the response of a fifth order digital elliptic

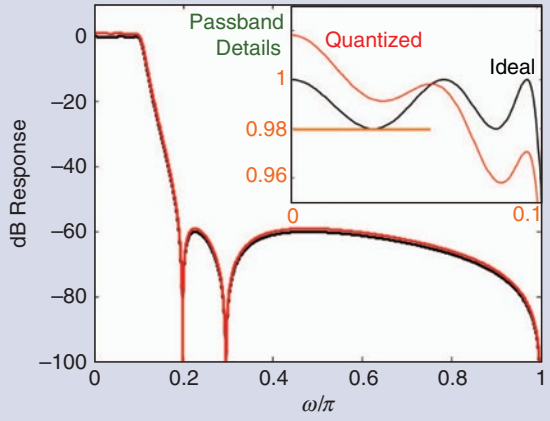


Figure 1. The effect of coefficient quantization. The magnitude response $|H(e^{j\omega})|$ of a 5th order elliptic lowpass filter is shown with 18 bit quantization (each multiplier is quantized to 18 bits). The direct-form structure [52], [54] is used. The red plot shows the response of the quantized structure whereas the black plot is the unquantized response. The passband details are shown in the inset. While the stopband response is nearly perfect even after quantization, it is clear that the passband response after quantization deviates significantly from the ideal.

P. P. Vaidyanathan is with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA. Sanjit K. Mitra is with the Department of Electrical and Computer Engineering at the University of California, Santa Barbara, CA. (e-mails: ppvnath@systems.caltech.edu, mitra@ece.ucsb.edu). *This work was supported in parts by the NSF grant CCF-1712633, the ONR grants N00014-17-1-2732, N00014-18-1-2390, and the California Institute of Technology.*

filter implemented in direct-form [16], [52], [54]. The ideal response is shown in black and the response with multiplier coefficients quantized to 18 bits is shown in red. Notice that the passband response (shown separately in the inset) deviates considerably from the ideal, even with 18 bits of precision for each multiplier coefficient. For higher order filters which have sharp cutoff and very small passband ripples, this effect is even more severe. The good news is that if the direct-form structure is replaced with a properly chosen structure, then these effects of quantization can be reduced to a considerable extent.

A. A Lesson Learned From Passive Electrical Filters

Historically, even before the advent of digital filters, it was well known that continuous time electrical filter circuits exhibited very low passband sensitivity (with respect to circuit element variations) if they are implemented as lossless (i.e., LC) circuits terminated at both ends appropriately with resistors. Such a doubly terminated lossless two-port is shown in Fig. 2(a). Define the filter transfer function as the voltage ratio $H(s) = 2Y(s)/X(s)$. With element values appropriately chosen, this can be designed to be a lowpass filter with response as in Fig. 2(b). It is found that such a filter exhibits low passband sensitivity with respect to element variations.

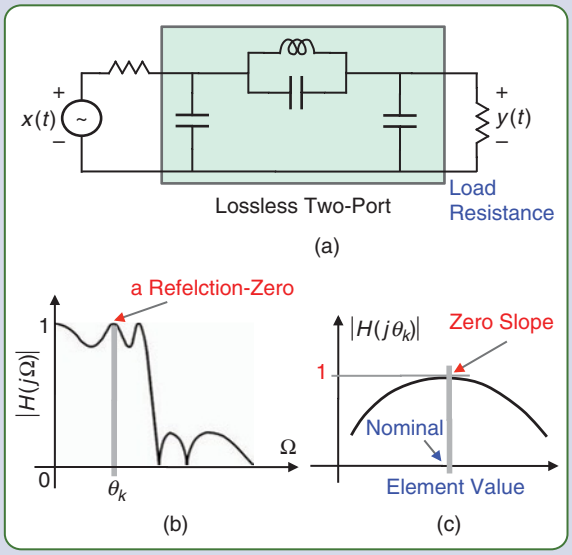


Figure 2. Fundamentals of low passband-sensitivity in *LCR* filters. (a) A lossless (LC) circuit, terminated at both ends with resistances. The resistances are such that maximum power is transferred from the source to the load at certain frequencies in the passband of the filter. (b) A typical lowpass filter response, realized as the ratio $H(s) = 2Y(s)/X(s)$. The passband maxima occur at the "reflection zeros" θ_k, where maximum power is transferred from the voltage source to the load resistance. (c) Variation of the response at $\Omega = \theta_k$ with respect to variation in a circuit element. The response can only decrease as the element value departs from nominal. This behavior was used by Orchard [55] to explain the low passband sensitivity of doubly terminated lossless two-ports.

An explanation for the low passband sensitivity was given by Orchard [55]: the two port is usually designed such that there is maximum transfer of power from the source $x(t)$ to the load $y(t)$ at the passband maxima. Thus, at a frequency $\omega = \theta_k$ in the passband (Fig. 2(b)), where the filter has maximum gain, there is maximum transfer of power. When a circuit element is perturbed, the transfer of power, hence the gain $|H(j\theta_k)|$, can only get smaller as demonstrated in Fig. 2(c). Thus the passband maxima exhibit low sensitivity with respect to element values. If there is a number of such maxima in the passband then the entire passband response has low sensitivity. A more quantitative explanation was given later in [56]. Incidentally, the frequencies θ_k are called **reflection zeros** because there is no power reflected back from the load resistance at these frequencies. Note that networks designed as above do not guarantee low *stop band* sensitivity.

The term low sensitivity can have multiple meanings. In this paper it is used to indicate the small sensitivity of the *magnitude response* in the *passband*. This is often quantified by the derivative of the passband magnitude response with respect to element values (as in the left hand side of Eq. (8)). The sensitivity of the phase response, or that of the response in the stop band will not be the focus here.

B. Fettweis's Vision

Fettweis recognized that this low sensitivity property of a doubly terminated lossless network can be inherited by a digital filter structure, if the structure is derived from the electrical network by an appropriate transformation. In his pioneering work in 1971, he achieved this [18], [19] by obtaining a digital equivalent for every circuit element (inductor, capacitor, resistor, open circuit, short circuit, voltage source, and so forth) by using the wave variable transformation (1) followed by the bilnear transformation [54]. In this process the quantities R_i, called the port resistances are chosen carefully so that, when the digital equivalents were interconnected, there were no *delay-free loops*. Fettweis developed the so-called series wave adaptor and parallel wave adaptor for the purpose of interconnecting digital equivalents of circuit elements [27].

To be specific, let us consider the case of an inductor L. When this is appropriately transformed, its digital equivalent is $-z^{-1}$ where z^{-1} represents a unit delay. To see this recall that the inductor is characterized by the

relation $V(s)=sLI(s)$. With the wave variables defined as $A(s)=V(s)+RI(s)$ and $B(s)=V(s)-RI(s)$, we have $B(s)=(sL/R-1)/(sL/R+1)A(s)$, With the free port-resistance chosen as $R=L$ this reduces to

$$B(s)=\frac{s-1}{s+1}A(s) \tag{2}$$

If we now use the bilinear transform $s=(1-z^{-1})/(1+z^{-1})$, then $(s-1)/(s+1)$ reduces to $-z^{-1}$ so that the digital equivalent of (2) becomes

$$B_d(z)=-z^{-1}A_d(z). \tag{3}$$

Thus an inductor transforms into $-z^{-1}$. Similarly a capacitor can be transformed into z^{-1}. When the doubly terminated lossless network of Fig. 2(a) is transformed using such digital equivalent building blocks, it results in the wave digital filter shown in Fig. 3. Notice the use of series and parallel adaptors for interconnecting the elements. The figure also shows the internal details of one of the adaptors. The main complexity and computational load of wave digital filters come from these adaptors.

As wave digital filters have been widely written about, we do not go into further details of the construction here. The interested reader will enjoy reading the original articles [18], [19], [27], or the excellent presentation in Antoniou's text book [3]. A short section on wave digital filters can also be found in Sec. XIII of [83] (chapter in an edited handbook), and will serve as an introduction for new readers.

As envisioned by Fettweis, wave digital filters indeed exhibited very low passband sensitivity. In addition, they also enjoyed freedom from parasitic oscillations or limit cycles, as shown in later papers by Fettweis and Meerkotter [26]. Wave digital filters were soon also extended to wave lattice filters [21], [30] and other variations. Wave filters for multirate applications have also been developed by Fettweis and Nossek [29]. A detailed overview article on wave filters, written by Fettweis himself, can be found in [23].

Wave digital filters have also been extended to the case of *multiple dimensions* [22], [28] but we shall not discuss those in our limited overview here. Many subtle aspects regarding passivity and stability of multidimensional filters are discussed in papers by Basu and Fettweis [6], [24], [25]. For papers focussing on multidimensional stability the reader is referred to [8], [9], [39], [67] and [60].

C. Wave Filters From Two-Port Viewpoint

Subsequent to the invention of wave digital filters, some researchers made efforts to simplify the procedure. In particular, considerable simplification could be obtained if the wave adaptors can be avoided, or implicitly incorporated without having to worry about cumbersome rules for interconnecting them. Swamy and Thyagarajan [68] came up with an ingenious way to do this. Their wisdom was to regard each circuit element itself as a two-port rather than a one-port as demonstrated in Fig. 4(a). Using this idea an LC ladder network can then be transformed directly into a "cascaded structure" of the form shown in Fig. 4(b). Here each rectangular box represents a 2×2 digital transfer matrix, also known variously as the **digital two-port** or **digital two-pair** [49]. It represents the digital equivalent of electrical elements such as inductors, capacitors, and even series or parallel LC circuits. Notice that the cascade in Fig. 4 is not a traditional cascade because the arrows are running in different directions, creating feedback loops. This sort of cascade is often called a **chain-cascade**. The reason for this name is that, in such a cascade, the so-called chain matrices (rather than transfer matrices) of the systems in cascade are multiplied. Please see Box 1 for details.

Each of these two-pairs in Fig. 4(b) is first-order (i.e., has one z^{-1} element) if it represents an L or a C element, and is second-order if it represents a series or parallel LC circuit. It was shown by Swamy and Thyagarajan that

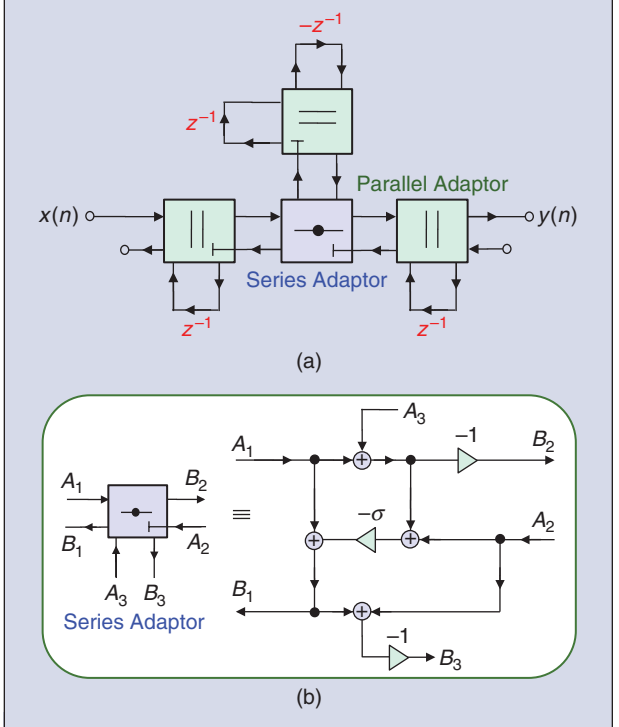


Figure 3. The wave digital filter obtained from the doubly terminated LC filter of Fig. 2. Details of a typical series adaptor used in wave digital filters are shown in the bottom. Parallel adaptors have a similar structure. For more details please see [18], [19], [27], or the text book [3], or Sec. XIII of [83].

LC ladder networks and more generally LCR circuits can be transformed into such a cascade of two-pairs. Furthermore, certain free parameters in the transformation can be selected such that delay free loops are avoided in the back to back interconnections. With this new type of wave digital filters we do not have to worry about the design of adaptors, as they are implicitly and automatically included in the two-ports of Fig. 4(b).

Box 1: Two Types of Cascaded Systems

A 2-input 2-output system has also been referred to as a *two-port* or a *two-pair*. With $\mathbf{x}(n) = [x_1(n) \quad x_2(n)]^T$ and $\mathbf{y}(n) = [y_1(n) \quad y_2(n)]^T$ denoting the input and output, there are two popular ways to describe an LTI two port. The *transfer matrix* and the *chain matrix* descriptions:

$$\begin{bmatrix} Y_1(z) \\ Y_2(z) \end{bmatrix} = \underbrace{\begin{bmatrix} T_{11}(z) & T_{12}(z) \\ T_{21}(z) & T_{22}(z) \end{bmatrix}}_{\text{transfer matrix } \mathbf{T}(z)} \begin{bmatrix} X_1(z) \\ X_2(z) \end{bmatrix},$$

$$\begin{bmatrix} X_1(z) \\ Y_1(z) \end{bmatrix} = \underbrace{\begin{bmatrix} A(z) & B(z) \\ C(z) & D(z) \end{bmatrix}}_{\text{chain matrix } \mathbf{\Pi}(z)} \begin{bmatrix} Y_2(z) \\ X_2(z) \end{bmatrix}$$

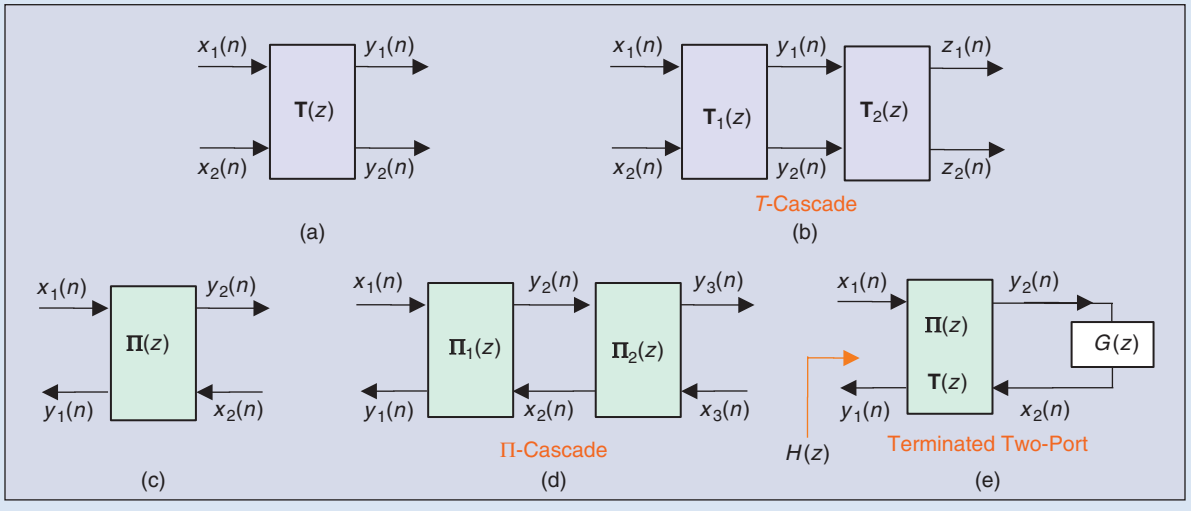
Depending on the description chosen it is convenient to show the inputs and outputs either as in (a) or as in (c) in the figure. The transfer matrix $\mathbf{T}(z)$ is convenient when two-ports are connected in a so-called ***T*-cascade** as shown in part (b). In this case the transfer matrix of the cascade is the product $\mathbf{T}(z) = \mathbf{T}_2(z)\mathbf{T}_1(z)$. The chain-matrix description is convenient when two-ports are connected in a so-called **Π-cascade** as shown in part (d). This interconnection generates new feedback loops and the description of the cascaded system in terms of transfer matrices becomes cumbersome. But the chain-matrix description becomes extremely convenient: with $\mathbf{\Pi}_k(z)$ denoting the chain matrices of the systems, the chain matrix of the Π-cascade is just the product $\mathbf{\Pi}(z) = \mathbf{\Pi}_1(z)\mathbf{\Pi}_2(z)$. The two descriptions are interrelated as follows: $T_{11} = C/A$, $T_{12} = \det \mathbf{\Pi}/A$, $T_{21} = 1/A$, $T_{22} = -B/A$ and similarly, $A = 1/T_{21}$, $B = -T_{22}/T_{21}$, $C = T_{11}/T_{21}$, $D = -\det T/T_{21}$ where the argument (z) has been omitted for simplicity.

Now consider part (e) in the figure where a two-port is "terminated" at one end by a transfer function $G(z)$. In this case, the transfer function $H(z) = Y_1(z)/X_1(z)$ can be expressed either in terms of the transfer parameters $T_{km}(z)$ or chain parameters $A(z), B(z), C(z), D(z)$ as follows:

$$H(z) = T_{11}(z) + \frac{T_{12}(z)\,T_{21}(z)\,G(z)}{1 - T_{22}(z)\,G(z)}, \quad \text{or equivalently}$$

$$H(z) = \frac{C(z) + D(z)\,G(z)}{A(z) + B(z)\,G(z)}$$

The chain matrix description has its origin in electrical circuit theory. *LCR* circuits in a ladder configuration can be conveniently expressed as a Π-cascade of two-ports where each two-port represents a series or parallel branch in the ladder. The chain matrix is therefore inherited into wave digital filters as seen explicitly from the work of Swamy and Thyagarajan (1975). It has also been used in direct synthesis of digital ladder filter structures by Mitra, Kamat, and Huey (1977). Later on it was also used extensively by Vaidyanathan and Mitra (1984) for the synthesis of structurally passive digital filters.



III. Direct Digital Synthesis

In the early to middle seventies, many other researchers besides Fettweis got interested in synthesis of digital filter structures inspired by *LC* network synthesis [10], [13], [49]. Many of these structures had qualitative similarities to *LC* ladder networks, but they were not necessarily designed to inherit specific properties such as low sensitivity or passivity. In 1977, Mitra, Kamat and Huey [50] proposed a way to synthesize digital transfer functions directly in the z-domain by extracting digital two-pairs (as in Fig. 4) in such a way that there is a degree reduction at each step in the extraction. (We will return to this in Fig. 7 again.) This procedure resulted in a number of new realizations for digital filters, but again, the two-pairs were not designed with any specific properties that would induce low sensitivity or passivity. However this basic idea of digital two-pair extraction, which realizes digital filters by successive order reduction, laid the foundation for future work which incorporated such robustness properties systematically into digital filter synthesis. More specifically, the approach introduced in [71] showed how to develop two-pair extraction methods to obtain digital filter structures with low sensitivity and other passivity properties, without recourse to continuous-time electrical circuits. This is based on a concept called structural passivity. This property is crucial to low sensitivity, and it can be incorporated directly into digital filter structures as explained next.

A. Structural Boundedness or Structural Passivity

Any digital filter structure is essentially an interconnection of delay elements, scalar multipliers, and two-input adders, as shown schematically in Fig. 5(a). Imagine now that we have a structure with the following special property: no matter what the values of the multipliers m_i are, the frequency response is always bounded by unity, that is, $|H(e^{j\omega})| \le 1$ for all ω. We say that such an implementation is **structurally bounded**, that is, the structural interconnection itself ensures that the frequency response never exceeds unity. The term **structurally passive** is also used for reasons described below.

In practice we constrain the multipliers m_i to belong to some reasonable range (such as, for example $|m_i| < 1$) as we shall indicate explicitly in the context of specific examples. In practice one also likes to make sure the transfer function remains stable. In order to be precise with these ideas, we introduce a number of important definitions here:

Definition 1.

Bounded transfer functions. A digital filter transfer function $H(z)$ is said to be *bounded* if it is stable (i.e., all poles are in $|z| < 1$) and $|H(e^{j\omega})| \le 1$ for all ω. Notice also the following definitions, properties, and remarks:

1) It can be shown that a stable rational transfer function $H(z)$ is bounded if and only if

$$\sum_n |y(n)|^2 \le \sum_n |x(n)|^2 \tag{4}$$

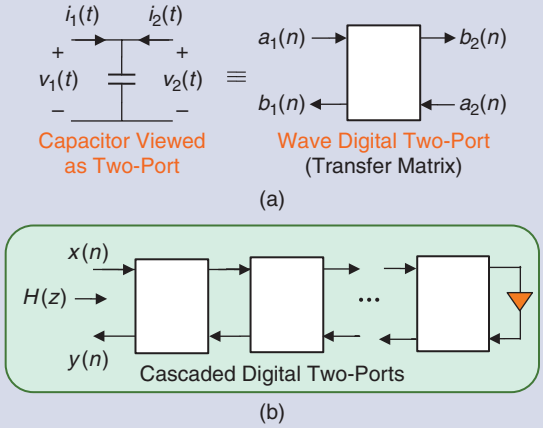


Figure 4. The wave digital filter synthesis method of Swamy and Thyagarajan [68]. (a) Each electrical element is regarded as a two-port as demonstrated, rather than as a one port. (b) The entire electrical circuit is transformed into a digital chain-cascaded network of 2×2 digital transfer matrices (two-ports). This avoids the need for explicit use of wave adaptors.

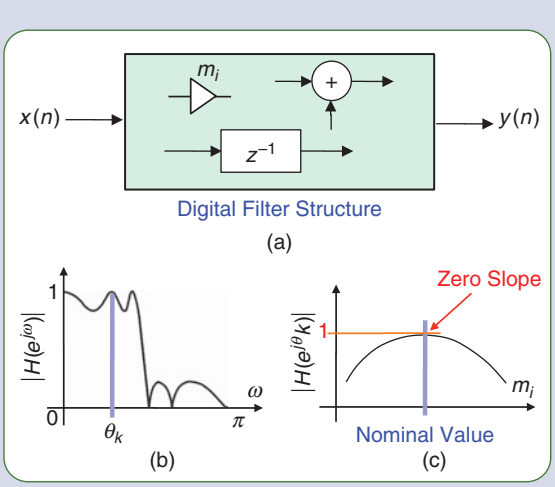


Figure 5. Structural boundedness and low passband sensitivity. (a) Any digital filter structure is an interconnection of delay elements, multipliers, and adders. (b) A typical lowpass response, with peak frequencies θ_k in the passband. (c) Variation of the response $|H(e^{j\theta_k})|$ with respect to a multiplier m_i. In a structurally bounded (or passive) system, the quantity $|H(e^{j\theta_k})|$ can only decrease as m_i deviates from its nominal value. This induces low passband sensitivity.

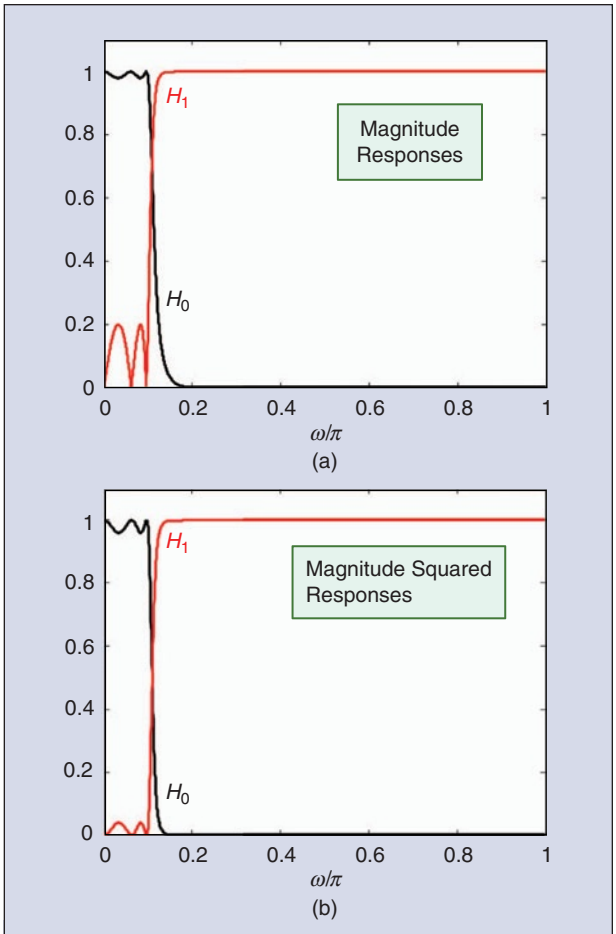


Figure 6. Responses of fifth order power complementary elliptic digital filters. (a) Magnitude responses, and (b) magnitude squared responses. Notice in (b) that the shapes of the ripples of the two filters are exactly complementary so that they add up to unity everywhere.

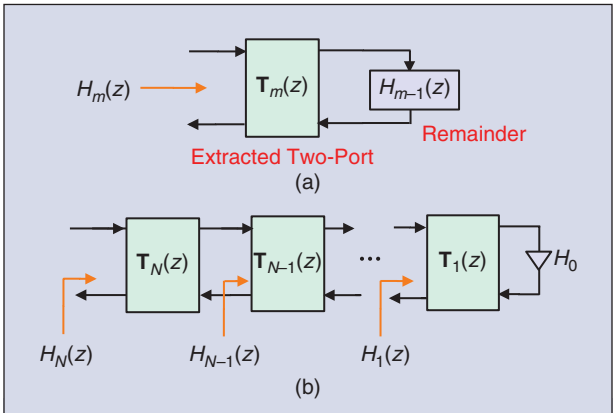


Figure 7. (a) The two-pair or two-port extraction step. Here the mth order transfer function $H_m(z)$ is implemented as a two-pair $\mathbf{T}_m(z)$ terminated at one end with a transfer function $H_{m-1}(z)$ of smaller order $m-1$. (b) Repeated extraction of two-pairs results in the realization of a scalar transfer function as a cascade of two-pairs terminated in a multiplier H_0.

where $y(n)$ is the output of $H(z)$ in response to $x(n)$. That is, the signal energy cannot be increased by the system; so a bounded system is also said to be *passive*.

2) A bounded transfer function with $|H(e^{j\omega})|=1$ for all ω is called **lossless** and is nothing but a stable **allpass** filter. In this case Eq. (4) holds with equality for all inputs $x(n)$.
3) A bounded transfer function is said to be *bounded real* or **BR** if all the filter coefficients are real i.e., the impulse response $h(n)$ is real. In this case $H(z)$ is real for real z. A lossless function with real filter coefficients is called a *lossless bounded real* or **LBR** function. It is nothing but a stable allpass filter with real coefficients.
4) An $M\times K$ transfer matrix $\mathbf{T}(z)$ is said to be lossless if it is stable (i.e., all entries $T_{km}(z)$ are stable), and furthermore $\mathbf{T}(e^{j\omega})$ is unitary for all frequencies:

$$\mathbf{T}^H(e^{j\omega})\mathbf{T}(e^{j\omega})=\mathbf{I}_K \quad \forall\omega \tag{5}$$

where the superscript H denotes transpose conjugation. If the lossless matrix $\mathbf{T}(z)$ also has real coefficients, then we say it is a *LBR* transfer matrix. Note that we require $M\geq K$ for (5) to hold. For the special case where $K=1$, $\mathbf{T}(z)$ becomes a column vector $\mathbf{T}(z)=[H_0(z)\,H_1(z)\ldots H_{M-1}(z)]^T$ and (5) implies

$$\sum_{k=0}^{M-1}|H_k(e^{j\omega})|^2=1 \tag{6}$$

which is also referred to as the **power complementary** property. ◊

Figure 6 demonstrates the meaning of the power complementary property for the case where $M=2$. If the elements of $\mathbf{T}(z)$ are rational functions of z, then the property (5) implies

$$\widetilde{\mathbf{T}}(z)\mathbf{T}(z)=\mathbf{I} \quad \forall z \tag{7}$$

where $\widetilde{\mathbf{T}}(z)=\mathbf{T}^H(1/z^*)$. The property (7) is called the **paraunitary** property. In short a rational lossless matrix is a stable and paraunitary matrix. The mathematical origin of this property can be traced back to **scattering matrices** in classical network theory in the context of lossless multiports [2], [7], [53]. Multidimensional extensions are also well-known, please see [5] and references therein.

B. Low Sensitivity Induced by Structural Boundedness

Now consider a digital lowpass filter with response as shown in Fig. 5(b). This is a bounded filter, with maximum

response of $|H(e^{j\omega})|=1$ at some frequencies θ_k in the passband. Assume this filter is realized using a structurally bounded implementation. In this implementation, the multipliers are such that $|H(e^{j\omega})|=1$ at $\omega=\theta_k$. Now, if a particular multiplier m_i is disturbed from its ideal value m_{i_0} (say due to quantization), then the response $|H(e^{j\theta_k})|$ can only decrease from the maximum of unity. We therefore have the behavior shown in Fig. 5(c). This shows that

$$\left.\frac{\partial|H(e^{j\theta_k})|}{\partial m_i}\right|_{m_i=m_{i_0}}=0 \tag{8}$$

That is, the sensitivity with respect to m_i is zero at the maxima $\omega=\theta_k$. Thus, the structure exhibits low passband sensitivity with respect to multipliers, especially if there are a number of maxima θ_k in the passband. Thus the behavior of a structurally bounded system is similar to that of a doubly terminated lossless two-port with maximum power transfer at the maximal points (reflection zeros) of the passband. The main point however is that structural boundedness can be directly achieved in the z-domain without recourse to electrical filters as we explain next. Like doubly terminated lossless electrical circuits, structural passivity does not guarantee low stop band sensitivity.

C. A Synthesis That Achieves Structural Boundedness

The basic step in the structurally bounded realization of a BR transfer function, as described in [71], is as follows: given an mth order BR function $H_m(z)$, we "extract" an LBR two-pair $\mathbf{T}_m(z)$ and a BR "remainder" $H_{m-1}(z)$ with smaller order $m-1$, such that $H_m(z)$ can be implemented as in Fig. 7(a). The conditions on $H_m(z)$ under which this is possible, as well as the details of the specific two-pairs $\mathbf{T}_m(z)$ to be used are described in [71]. Since the remainder $H_{m-1}(z)$ remains BR, we can repeat this extraction process until the final remainder H_0 is a constant BR function (i.e., $-1\le H_0\le 1$). Thus starting from an Nth order BR function $H_N(z)$, we can obtain the chain-cascaded structure shown in Fig. 7(b). While it is not obvious, it can be shown that such a synthesis is always possible for classical transfer functions (elliptic, Cheybyshev, and Butterworth filters). Broadly speaking, two types of LBR two-pair building blocks are necessary for this: first-order and second-order building blocks. Each of these comes with some minor variations depending on the details of the transfer function to be synthesized as elaborated in Tables 2, 3, and 4 of [71]. A typical first order LBR two-pair involved in the synthesis takes the form

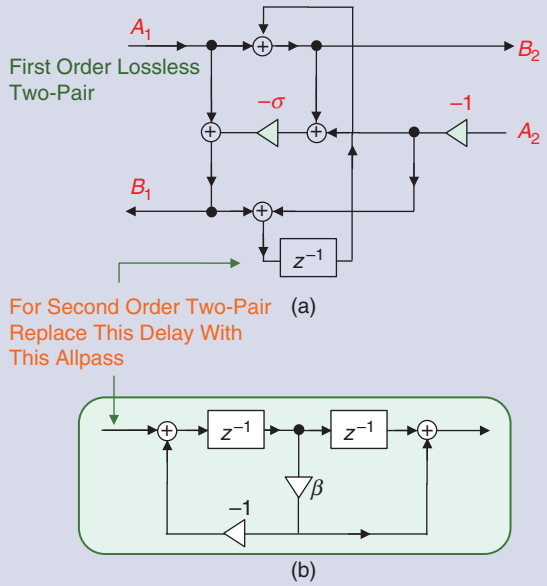


Figure 8. (a) Example of a first order lossless two-port or two-pair developed in [71]. Notice similarity to series wave adaptor (Fig. 3), with third port terminated by a delay. (b) One way to obtain a second order lossless two-port, is to replace the delay element z^{-1} with an allpass filter, as indicated.

$$\mathbf{T}(z)=\frac{1}{1+\sigma z^{-1}}\begin{bmatrix}1-\sigma & \sqrt{\sigma}(1+z^{-1})\\ \sqrt{\sigma}(1+z^{-1}) & (\sigma-1)z^{-1}\end{bmatrix} \tag{9}$$

where $0\le\sigma<1$ so that the pole is inside the unit circle and furthermore $\sqrt{\sigma}$ is real. It is readily verified that $\widetilde{\mathbf{T}}(z)\mathbf{T}(z)=\mathbf{I}$ so that $\mathbf{T}(z)$ is LBR. Figure 8(a) shows an implementation of the first order two-pair (9). The multipliers $\sqrt{\sigma}$ do not appear because they can be removed by a denormalization process which does not change the transfer functions $H_m(z)$. To be more specific, if a two-pair $\mathbf{T}_m(z)$ has the general form

$$\begin{bmatrix}T_{11}(z) & T_{12}(z)\\ T_{21}(z) & T_{22}(z)\end{bmatrix} \tag{10}$$

then only the product $T_{12}(z)T_{21}(z)$ matters in determining the transfer functions $H_m(z)$. So replacing $T_{12}(z)$ with $\alpha T_{12}(z)$ and $T_{21}(z)$ with $T_{21}(z)/\alpha$ where $\alpha=\sqrt{\sigma}$ or $\alpha=1/\sqrt{\sigma}$ gets rid of $\sqrt{\sigma}$. Fig. 8(a) is one such denormalized structure.

A typical second order LBR two pair arising in the synthesis of BR functions is obtained simply by replacing z^{-1} in Eq. (9) with the allpass function

$$z^{-1}\frac{\beta+z^{-1}}{1+\beta z^{-1}} \tag{11}$$

where $-1<\beta<1$. Please see Fig. 8(b). Some other minor variations of these first and second order LBR two-pairs

Historically the mathematics of the lattice structure can be traced back to the mathematical works of Schur and Szego in the early 1900s, and the work of Levinson.

are tabulated in [71] and are sufficient to realize a large class of BR transfer functions in the form of Fig. 7(b).

How does this cascade achieve structural boundedness? If the multipliers σ_i and β_i are restricted to their specific ranges in spite of quantization (i.e., $0 \le \sigma_i < 1$ and $-1 < \beta_i < 1$) then each two-port remains LBR. If the rightmost multiplier H_0 is quantized such that the property $-1 \le H_0 \le 1$ continues to be respected, then all the transfer functions $H_m(z)$ will remain BR in spite of multiplier quantization. Thus boundedness of $H_N(z)$ can be structurally enforced.

IV. Generality of the Structurally Passive Approach

The synthesis of a BR transfer function by extraction of LBR building blocks gives rise to a number of well known low sensitivity structures as special cases. In fact, notice the similarity between the LBR two-pair shown in Fig. 8(a) and the wave adaptor shown Fig. 3. This similarity is not coincidental. The direct digital synthesis described in Sec. 3.3 does give rise to the type of wave digital filters developed by Swamy and Thyagarajan (Sec. 2.3) as special cases; please see [71].

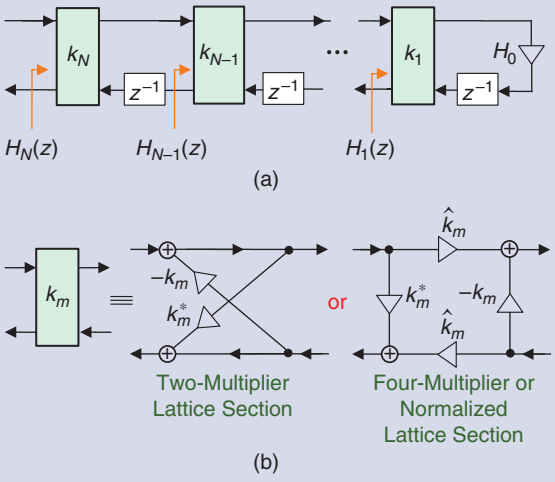


Figure 9. (a) The Gray-and-Markel recursive lattice structure for allpass filters. (b) Two possible choices for the lattice sections. The transfer functions $H_k(z)$ are the same regardless of which of these sections is used. This lattice is also known as the linear-prediction lattice because it has its origin in the theory of linear prediction, and was extensively studied in the context of speech coding.

A. The Gray-Markel Allpass Lattice

Another special case is the well-known Gray and Markel lattice structure for allpass filters [32]. Please see Box 2 for a review of allpass filters; these filters have many applications [61], including low sensitivity implementations [77] and frequency transformations [12].

The allpass lattice structure is shown in Fig. 9. In this structure the lattice coefficients k_m satisfy $|k_m| < 1$, and

$$\hat{k}_m = \sqrt{1 - |k_m|^2} \tag{12}$$

It can be shown that the transfer function $H_N(z)$ is stable and **allpass**, that is, $|H_N(e^{j\omega})| = 1$ for all ω. In fact any stable rational allpass filter can be implemented this way. The coefficients k_m are real for real-coefficient allpass filters.

This structure was derived independently in 1973 without reference to either the wave filter approach or structural passivity [48], [57], [90]. In fact, historically, the mathematics of the structure can be traced back to the mathematical works of Schur and Szegö in early 1900s [62], [63], [70] and the work of Levinson [44]. It was developed further in the signal processing literature in the 1970s, in the context of linear prediction theory [4], [38], [43], [48], [57], [90]. Please also see the classic tutorial articles by Kailath [40] and Makhoul [45] in this context.

Now, since $H_N(z)$ is allpass, it is in particular a bounded function, and it can be synthesized in the form of a chain-cascade by extracting lossless two-ports as described in Sec. 3.3. There are many choices of lossless two ports that make this synthesis possible. One specific synthesis, described in Sec. 3.4.3 of [88], yields the specific structure of Fig. 9. More details can be found in [81]. Thus the Gray-Markel lattice can be regarded as a special case of the lossless two-port extraction method. The transfer matrix of each lossless two-port in this example takes the form

$$\mathbf{T}_m = \begin{bmatrix} k_m^* & \hat{k}_m \\ \hat{k}_m & -k_m \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 0 & z^{-1} \end{bmatrix} \tag{13}$$

The constant matrix above is the four-multiplier or normalized building block [33] shown in Fig. 9(b). There are many denormalized versions of the lattice, as explained in detail in [88].

In addition to structural passivity, this implementation also involves an **internal passivity** which leads to

Box 2: Allpass Functions

Allpass filters are fundamental building blocks in signal processing. A digital filter $H(z)$ is said to be allpass if $|H(e^{j\omega})|=1$ for all ω, that is $H(e^{j\omega})=e^{j\phi(\omega)}$. A rational allpass filter has the form

$$H(z)=\frac{b_N^*+b_{N-1}^*z^{-1}+\cdots+b_1^*z^{-(N-1)}+b_0^*z^{-N}}{b_0+b_1z^{-1}+b_2z^{-2}+\cdots+b_Nz^{-N}}=\frac{z^{-N}\tilde{B}(z)}{B(z)}$$

where $\tilde{B}(z)=B^*(1/z^*)$. This notation is equivalent to replacing the coefficients b_k by their complex conjugates, and replacing z with $1/z$. For a rational transfer function the allpass property can be rewritten as $\tilde{H}(z)H(z)=1$ for all z. Allpass filters are used in phase equalization, and in the implementation of certain filters. For example, as reviewed in this article, classical Butterworth, Chebyshev, and elliptic filters can be expressed as a *sum of two allpass filters*, leading to a structurally passive implementation with low passband sensitivity. Such structures also have very few multipliers compared to direct-form and other structures. The nonzero poles p_k and zeros z_k of a rational allpass filter have a reciprocal symmetry: $p_k=1/z_k^*$.

In fact, for a causal stable rational allpass function of order ≥ 1, a curious symmetry with respect to the unit circle, called the *modulus property* holds:

$$|H(z)|\begin{cases}<1 & \text{for } |z|>1\\ >1 & \text{for } |z|<1\\ =1 & \text{for } |z|=1\end{cases}$$

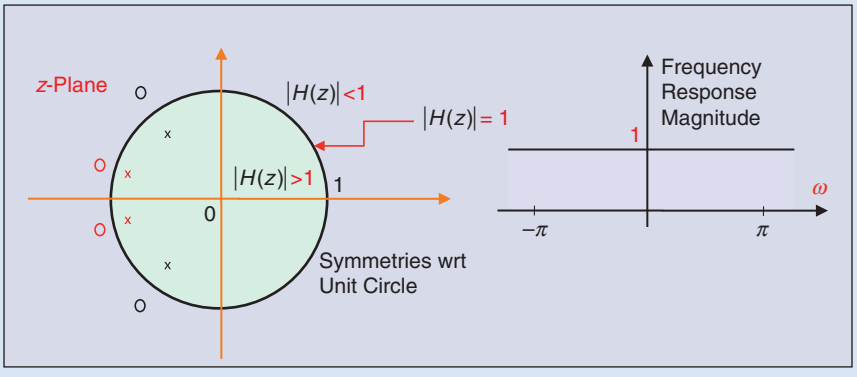
This is at the heart of the derivation of lattice structures and stability test procedures based on allpass systems as elaborated by Vaidyanathan and Mitra (1987). These symmetries with respect to the unit circle are summarized in the figure. Allpass filters are also very effective in the implementation of notch and antinotch filters. Many efficient structures exist for allpass filters such as the Gray and Markel lattice (1973), and the Mitra and Hirano class of structures (1974). A detailed review of allpass functions can be found in Regalia, Mitra, and Vaidyanathan (1988). An early application of allpass filters for frequency transformations was developed by Constantinides (1970). The allpass property can be generalized to MIMO systems as follows: an $M\times N$ transfer matrix $\mathbf{T}(z)$ is allpass if it is unitary on the unit circle, that is,

$$\mathbf{T}^H(e^{j\omega})\mathbf{T}(e^{j\omega})=\mathbf{I}_N$$

for all ω. This requires $M\geq N$. For rational transfer matrices this implies the *paraunitary* property: $\tilde{\mathbf{T}}(z)\mathbf{T}(z)=\mathbf{I}_N$ for all z. Here $\tilde{\mathbf{T}}(z)=\mathbf{T}^H(1/z^*)$. If $\mathbf{y}(n)$ is the output of a stable paraunitary system in response to input $\mathrm{x}(n)$, then

$$\sum_n y^H(n)y(n)=\sum_n x^H(n)\mathrm{x}(n)$$

That is, the output energy is equal to the input energy. So, stable paraunitary matrices and allpass filters are called *lossless* systems. Historically, lossless systems had a fundamental role in circuit and system theory as elaborated by Belevitch (1968) and by Anderson and Vongpanitlerd (1973). Paraunitary matrices arise in the cascaded synthesis of digital filters with structural passivity. For the special case where $N=1$, $\mathbf{T}(z)$ is a column vector with components $H_k(z)$, and the allpass property becomes $\Sigma_{k=0}^{M-1}|H_k(e^{j\omega})|^2=1$, which is the *power complementary* property. There is a systematic way to factorize FIR paraunitary matrices in terms of planar rotations and delay elements. These are summarized in the review paper by Vaidyanathan and Doğanata (1989). Paraunitary matrices also arise in the design of orthonormal digital filter banks. Please see Vaidyanathan (1993) for details.



Thus, wave filters, orthogonal filters, and cascaded lattice structures are nicely unified by the structurally passive synthesis methods which use LBR building blocks.

many useful properties, including *suppression of limit cycle oscillations* [34], [76]. The importance of this internal passivity in suppression of limit cycles has also been established independently in the context of wave digital filters [20], [26]. Further generalizations as well as simplifications can be found in [76], [79].

B. Orthogonal Digital Filters and Rotation Operators

Before we discuss further examples it is useful to introduce the planar rotation operator which turns out to be an important building block for many types of digital filter structures. Thus, consider the matrix

$$\mathbf{\Theta}_m = \begin{bmatrix} \cos\theta_m & \sin\theta_m \\ -\sin\theta_m & \cos\theta_m \end{bmatrix} \tag{14}$$

and the operation $\mathbf{y} = \mathbf{\Theta}_m \mathbf{x}$. It is readily shown that $\mathbf{y}$ is the clockwise rotated version of $\mathbf{x}$, by the angle θ_m (page 290, [88]). This operator is therefore called the **planar rotation** operator, and is schematically denoted as shown in Fig. 10(a). It is also known as the *Givens rotation* operator or the *cordic* processor [31], [37], [42]. As an example of how this operator arises, consider the allpass lattice structure with the four-multiplier or normalized building block (Fig. 9). If the filter has real coefficients, then k_m are real and we can write $k_m = \cos\theta_m$ and $\hat{k}_m = \sqrt{1-k_m^2} = \sin\theta_m$ for some real θ_m so that the computational blocks become

$$\begin{bmatrix} k_m & \hat{k}_m \\ \hat{k}_m & -k_m \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}}_{\mathcal{R}} \underbrace{\begin{bmatrix} \cos\theta_m & \sin\theta_m \\ -\sin\theta_m & \cos\theta_m \end{bmatrix}}_{\mathbf{\Theta}_m} \tag{15}$$

Here $\mathcal{R}$ is just a reflection operator, as it merely reverses the sign of the y-component. Thus, the allpass filter can be implemented entirely in terms of planar rotations as the computational units.

Similarly it has been shown [75] that the first order LBR two-pair of Fig. 8(a) can be rearranged in terms of two planar rotations as shown in Fig. 10(b). In fact, any BR transfer function, synthesized in terms of the first and second order LBR two-pairs of Fig. 8 can be expressed in terms of planar rotations as the only computational units [75]. Digital filter structures which can be expressed entirely in terms of rotation operators were first noticed by Deprettere and Dewilde in the context of a family of structures called **orthogonal filter** structures [15], [58], which enjoy several robustness properties under quantization. It should also be mentioned here that paraunitary matrices can be neatly factorized into planar rotations (or other fundamental unitary blocks such as Householder matrices) and delay elements [17], [84]–[86], [88].

The preceding discussions show that the Gray-Markel lattice structures (Fig. 9) and the structurally passive cascaded structures (Fig. 7(b) with building blocks as in Fig. 8) can be expressed as orthogonal digital filter structures. Thus, wave filters, orgthogonal filters, and cascaded lattice structures are nicely unified by the structurally passive synthesis methods which use LBR building blocks.

We conclude by mentioning that the lossless two-port extraction approach of Sec. 3.3 has also been extended to transfer functions with multiple inputs and multiple outputs (MIMO). Figure 11(a) shows an example of a single-input multi-output transfer matrix with transfer function $\mathbf{H}_N(z)$. Here the transfer matrices $\mathbf{T}_m(z)$ are MIMO lossless transfer matrices, that is, they are stable and satisfy $\widetilde{\mathbf{T}}_m(z)\mathbf{T}_m(z) = \mathbf{I}$. It can be shown that if $\mathbf{H}_N(z)$ is SIMO lossless, it can be synthesized in this form by using the lossless multiport extraction approach [75]. A special case of this is the beautiful family of single-input

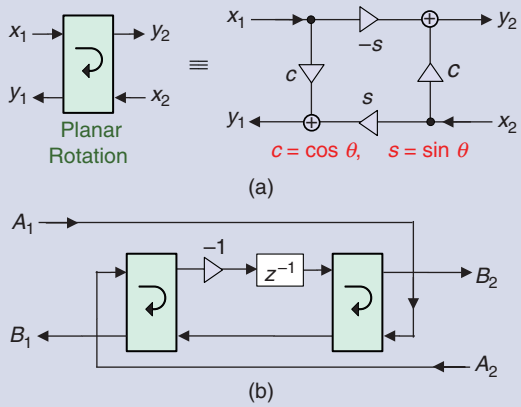


Figure 10. (a) The planar rotation operator. This rotates the vector $\mathbf{x} = [x_1 \;\; x_2]^T$ clockwise by an angle θ to produce $\mathbf{y} = [y_1 \;\; y_2]^T$. This is also known as the Givens rotation operator [31], or the cordic processor [37], [42]. (b) Implementation of the first order LBR two-port of Fig. 8(a) using planar rotation operators.

two-output lattice structures developed first by Rao and Kailath in 1984 [59] shown in Fig. 11(b). In this structure the matrices $\mathbf{R}_k$ are constant unitary matrices, and the transfer matrix $[H_N(z) \;\; G_N(z)]^T$ is lossless. That is, $H_N(z)$ and $G_N(z)$ are stable and satisfy

$$\tilde{H}_N(z)H_N(z) + \tilde{G}_N(z)G_N(z) = 1 \tag{16}$$

The above property implies the power complementary property $|H_N(e^{j\omega})|^2 + |G_N(e^{j\omega})|^2 = 1$. Thus, given any BR transfer function $H_N(z)$ we can always find its power complementary partner $G_N(z)$, and realize the pair as in Fig. 11(b). It can be shown in this specific case [75] that the 3×3 unitary matrices $\mathbf{R}_k$ can be implemented using two planar rotations each, as shown in Fig. 11(c). This is a structurally passive implementation of the BR function $H_N(z)$ in the sense that, regardless of the angular values of the rotations the transfer functions remain BR. In particular, the structure exhibits low passband sensitivity as explained in Sec. 3.2.

V. Further Examples of Structurally Passive Implementations

In this section we review a number of structurally passive implementations and demonstrate their low sensitivity properties. These methods are quite simple and can be understood independently in the z-domain without any background on circuit theory or electrical filters.

A. Parallel-Allpass Implementations

Consider Fig. 12 where $A_0(z)$ and $A_1(z)$ are stable rational allpass filters and $H_0(z)$ and $H_1(z)$ are obtained by adding and subtracting the outputs of the allpass filters as shown. It turns out that a large class of IIR digital filters, including Butterworth, Chebyshev, and elliptic filters, can be implemented in this way. This result is known in classical continuous-time filter theory and it is implicit in the design of wave lattice digital filters pioneered by Fettweis [21], [30]. However, the result is more general, and it can be proved quite easily and directly without reference to continuous-time circuit theory [77]. Thus, Theorem 3.6.1 in [88] establishes some sufficient conditions on $H_0(z)$ and $H_1(z)$ which allow their implementation as in Fig. 12(a). There are many special cases of filters which satisfy these sufficient conditions. For example if $H_0(z)$ is an odd order lowpass Butterworth, Chebyshev, or elliptic filter, it satisfies the conditions of the above theorem, and it can be expressed as

$$H_0(z) = \frac{A_0(z) + A_1(z)}{2} \tag{17}$$

where $A_0(z)$ and $A_1(z)$ are real-coefficient, stable, allpass filters. That is, they have the form [88]

$$A_k(z) = \frac{a_{k,n_k} + a_{k,n_k-1}z^{-1} + \cdots + z^{-n_k}}{1 + a_{k,1}z^{-1} + \cdots + a_{k,n_k}z^{-n_k}} \tag{18}$$

(Please see Box 2 for a review of allpass filters.) There are systematic ways to identify the coefficients of the

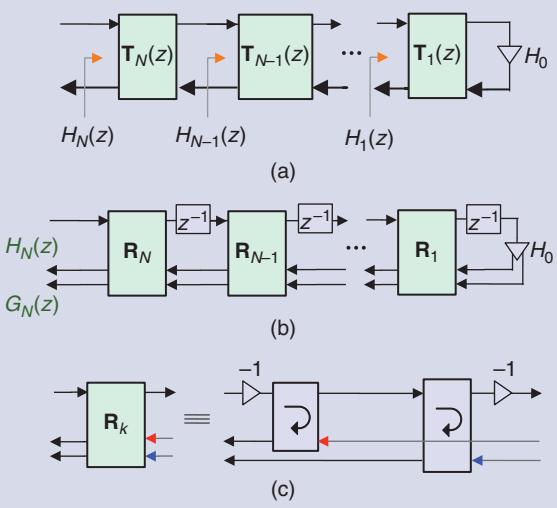


Figure 11. (a) The two-port extraction approach extended to single-input multi-output systems. (b) Example of a single-input two-output lattice, generating an IIR allpass vector, that is, an IIR power complementary pair $[H_N(z) \;\; G_N(z)]^T$. (c) Implementation of each building block using two planar rotations. The example in (b), (c) was first developed by Rao and Kailath in a pioneering work in the 1980s [59].

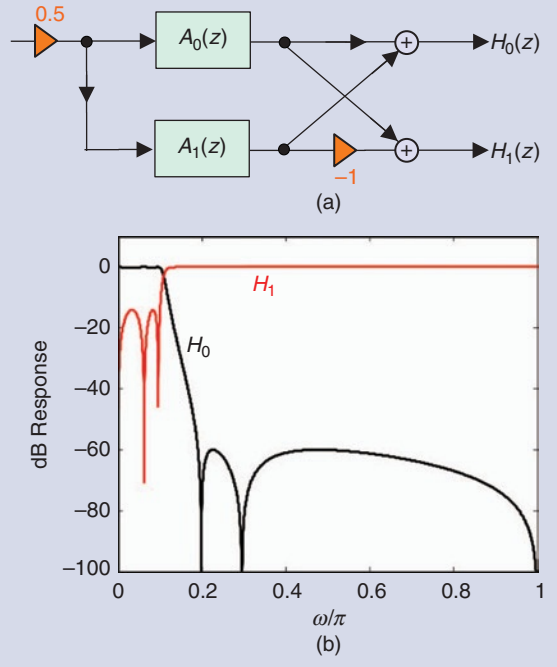


Figure 12. (a) The parallel allpass structure to implement a power complementary pair of bounded real transfer functions. (b) Example of filter responses.

allpass filters starting from the coefficients of $H_0(z)$ [77], [88]. With $A_k(z)$ identified, the filter

$$H_1(z) = \frac{A_0(z) - A_1(z)}{2} \tag{19}$$

turns out to be a highpass filter of the same kind (Butterworth, Chebyshev, or elliptic). From (17) and (19) it is easy to verify that the two filters are power complementary:

$$\left|H_0(e^{j\omega})\right|^2 + \left|H_1(e^{j\omega})\right|^2 = 1 \tag{20}$$

This is demonstrated in Fig. 12(b) where the filters are fifth order elliptic filters. The implementation of Fig. 12 is called the **parallel-allpass** implementation or sum-of-allpass implementation.

A similar implementation is possible for even-order Butterworth, Chebyshev, and elliptic lowpass filters, but $A_0(z)$ has complex coefficients $a_{k,i}$, and the coefficients of $A_1(z)$ are the conjugates of those of $A_0(z)$; see [80] for details. In this case $H_0(z)$ can be realized by taking the real part of the output of $A_0(z)$, and $H_1(z)$ realized by taking the imaginary part. In short, a single **complex allpass filter** can be used to implement the pair $H_0(z), H_1(z)$.

We now argue that Fig. 12(a) gives rise to a structurally passive implementation. While there exist many structures for implementation of allpass filters [32], [51], [61], [69], the Gray-Markel lattice is especially attractive in this context. If $A_i(z)$ are implemented using the Gray-Markel allpass lattice of Fig. 9, then as long as the quantized multipliers k_m continue to satisfy $|k_m| < 1$, the filters remain allpass as well as stable [81]. Thus, even when the multipliers are quantized $H_0(z)$ and $H_1(z)$ continue to be a sum and difference of two stable allpass filters as in Eqs. (17), (19). Since $|A_i(e^{j\omega})| = 1$ it is obvious that $|H_k(e^{j\omega})| \le 1$ which proves structural boundedness of $H_0(z)$ and $H_1(z)$. As explained in Sec. 3.2 these structures therefore enjoy low passband sensitivity.

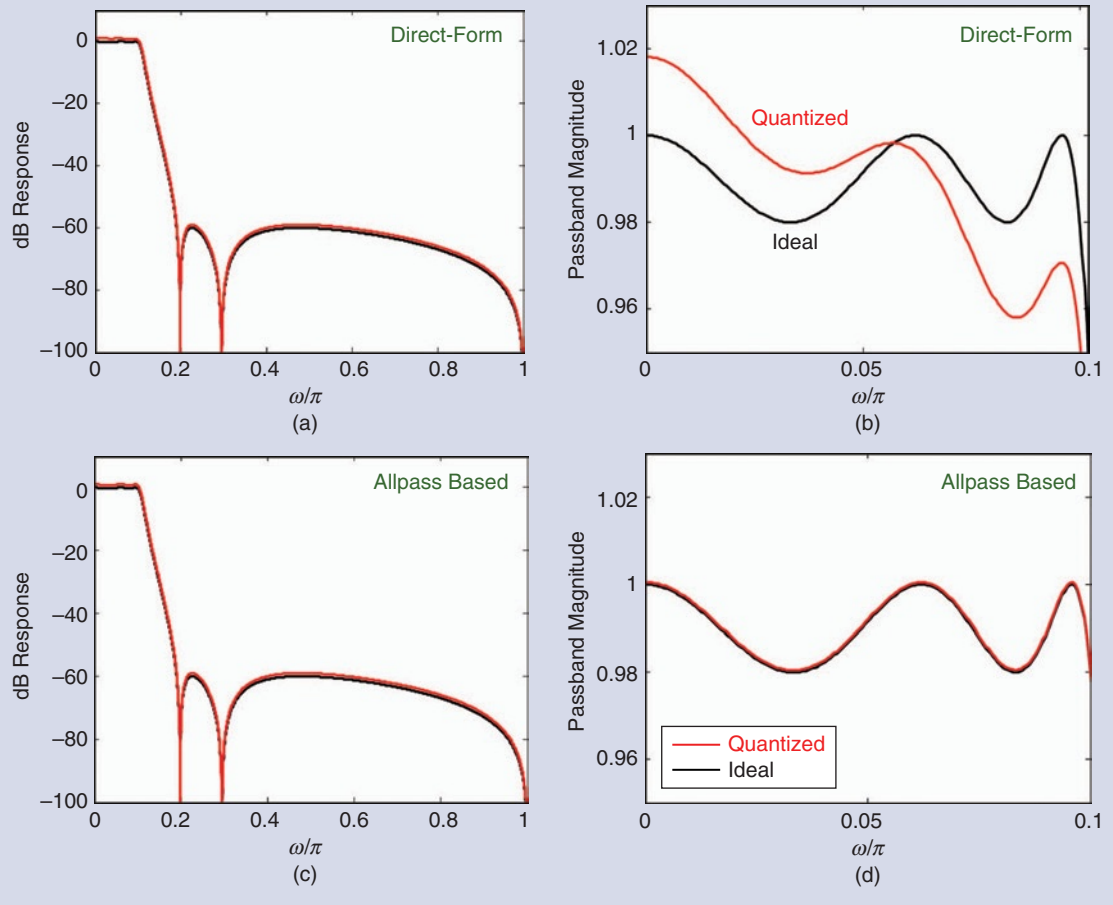


Figure 13. Responses of the direct-form structure and the parallel-allpass based structure under quantization. A fifth order IIR elliptic filter is simulated, and coefficients are quantized to 18 bits. The responses of quantized structures are shown in red, and responses of unquantized structures are in black. Notice that the parallel-allpass based system (structurally passive system) has very low passband sensitivity: the quantized response is indistinguishable from ideal.

In short, *we get two Nth order filters $H_0(z)$ and $H_1(z)$ at the total cost of only N multipliers!*

In addition to low sensitivity, the implementation Fig. 12 is also amazingly economic in terms of computational complexity. For example, assume $H_0(z)$ is an Nth order lowpass elliptic filter with odd N. Then the allpass filters have orders n_0 and n_1 where $n_0+n_1=N$. Each allpass filter can be implemented using a lattice structure as in Fig. 9. Now, instead of using the two-multiplier or four-multiplier lattice sections in Fig. 9(b), it is always possible to use one-multiplier sections (see Fig. 3.4-11 of [88]). If we do this then $A_k(z)$ requires only n_k multipliers, so that the entire implementation of Fig. 12 requires only N multipliers where N is the order of each filter $H_k(z)$. In short, *we get two Nth order filters $H_0(z)$ and $H_1(z)$ at the total cost of only N multipliers!* Indeed, this is *one of the most efficient ways* to implement Butterworth, Chebyshev and elliptic filters.

To demonstrate low sensitivity, consider a 5th order elliptic lowpass filter $H_0(z)$. In Fig. 13 we show the magnitude response of $H_0(z)$ with the quantized direct-form structure [54], and the quantized parallel allpass structure of Fig. 12(a). The responses of quantized structures are shown in red, and responses of unquantized structures are in black. For both structures, the dB plot of the entire response is shown, and the details of the passband region is shown separately. We have used 18 bits per multiplier coefficient in both structures. While both structures perform satisfactorily in the stopband, the passband response of the quantized direct-form deviates significantly from the ideal. In contrast, the quantized response of the structurally passive implementation (Fig. 12(a)) is nearly perfect in the passband as well, demonstrating very low passband sensitivity.

It is well known that if the Gray-Markel lattice structure is used to implement the allpass filters, then limit cycle oscillations can be suppressed [34], and furthermore, the roundoff noise gain is small [33]. Thus, the structurally passive implementation of Fig. 12(a) enjoys a number of robustness properties in addition to its computational economy. A special case of (17) where $A_0(z)=1$ is very useful for the design of notch and anti-notch filters [89].

B. The FIR Power Complementary Lattice

Consider Fig. 14(a) which is a cascaded lattice structure. Unlike in the earlier cascaded structures (e.g., Figs. 7 and 9), there are no feedback loops here. So, this is a **nonrecursive** or FIR lattice. The internal details of the lattice sections are shown in Fig. 14(b). In this figure we use the notations

$$c_m=\cos\theta_m,\quad s_m=\sin\theta_m \tag{21}$$

So the building blocks are planar rotations or denormalized versions of such rotations. This structure was introduced in [78] and has a number of interesting properties. First, the two transfer functions are $H_0(z)$ and $H_1(z)$ are guaranteed to be power complementary that is, $|H_0(e^{j\omega})|^2+|H_1(e^{j\omega})|^2=1$ regardless of the choice of the angles θ_m. (If denormalized lattice sections are used, then $|H_0(e^{j\omega})|^2+|H_1(e^{j\omega})|^2=c$ for some constant $c>0$). Secondly, given any pair of power complementary FIR filters $H_0(z)$ and $H_1(z)$ (with real coefficients), they can always be implemented using this lattice structure, by choosing the planar rotation angles θ_m appropriately. Now assume that we are given some FIR filter $H_0(z)$ with real coefficients and normalized such that $|H_0(e^{j\omega})|\le 1$, i.e., we are given an FIR BR function $H_0(z)$. Then we can always find an FIR BR $H_1(z)$ such that $\{H_0(z),H_1(z)\}$ is power complementary. For this we simply take $H_1(z)$ to be any spectral factor of $|H_1(e^{j\omega})|^2\triangleq 1-|H_0(e^{j\omega})|^2$. Then we can implement the pair as in Fig. 14. *This shows that we can obtain this cascaded lattice implementation for any FIR BR filter $H_0(z)$.*

Now, given such an implementation, if the angles θ_m in the rotations are perturbed, the power complementary property is not affected, and therefore the property $|H_0(e^{j\omega})|\le 1$ continues to hold. In this sense the

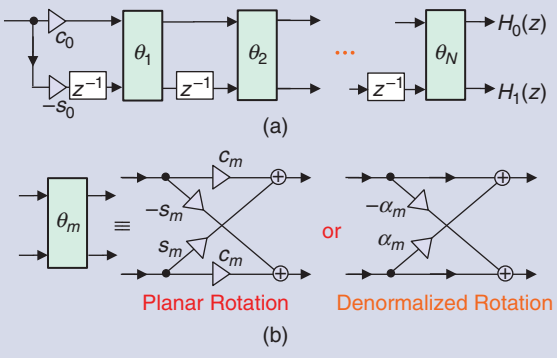


Figure 14. (a) The lattice structure for an FIR power complementary pair $[H_0(z),H_1(z)]$ [78]. (b) Details of the building blocks. Each block is a planar rotation operator. It can also be replaced by a denormalized section with two multipliers as shown.

implementation is structurally passive and therefore enjoys low passband sensitivity. In practice even the lattice with the denormalized sections shown in Fig. 14(b) exhibits low passband sensitivity. To demonstrate this, we consider a 60th order linear phase lowpass equiripple filter $H_0(z)$ designed using the McClellan-Parks algorithm [54], and implement it using the lattice structure (using the algorithm presented in [78]. We use the denormalized (two-multiplier) lattice sections of Fig. 14(b) and quantize the lattice coefficients α_m to 8 bits. We compare the resulting frequency responses with those of the direct form structure with multipliers quantized to 8 bits as well. Fig. 15 shows the filter magnitude responses for these implementations. The responses of quantized structures are shown in red, and responses of unquantized structures are in black. For both structures, the dB plot of the entire response is shown, and the details of the passband region is shown separately. While both structures perform satisfactorily in the stopband, the passband response of the quantized direct-form deviates significantly from the ideal. In contrast, the quantized response of the structurally passive implementation (Fig. 14(a)) is nearly perfect in the passband as well, demonstrating very low passband sensitivity.

The FIR lattice structure Fig. 14 is called the FIR power complementary lattice or the **FIR structurally passive lattice**. Readers familiar with the FIR linear prediction lattice or **LPC lattice** might wonder what the difference is. The linear-prediction lattice also has an appearance similar to Fig. 14 with two-multiplier lattice sections, but the minus sign on the α_m is not there, and furthermore, $|\alpha_m| < 1$. In terms of theoretical properties, this is a major difference. The FIR lattice structure of Fig. 14 can realize arbitrary BR $H_0(z)$. But the LPC lattice cannot be used to realize arbitrary FIR filters. It is typically used to realize prediction filters $H_0(z)$ with all zeros strictly inside the unit circle (minimum-phase filters). The filter $H_1(z)$ in an LPC lattice is not power complementary to $H_0(z)$, but rather, it is the mirror image polynomial $H_1(z) = z^{-N} H_0^*(1/z^*)$. So, in the LPC lattice, $H_1(z)$ has all its zeros *outside* the unit circle.

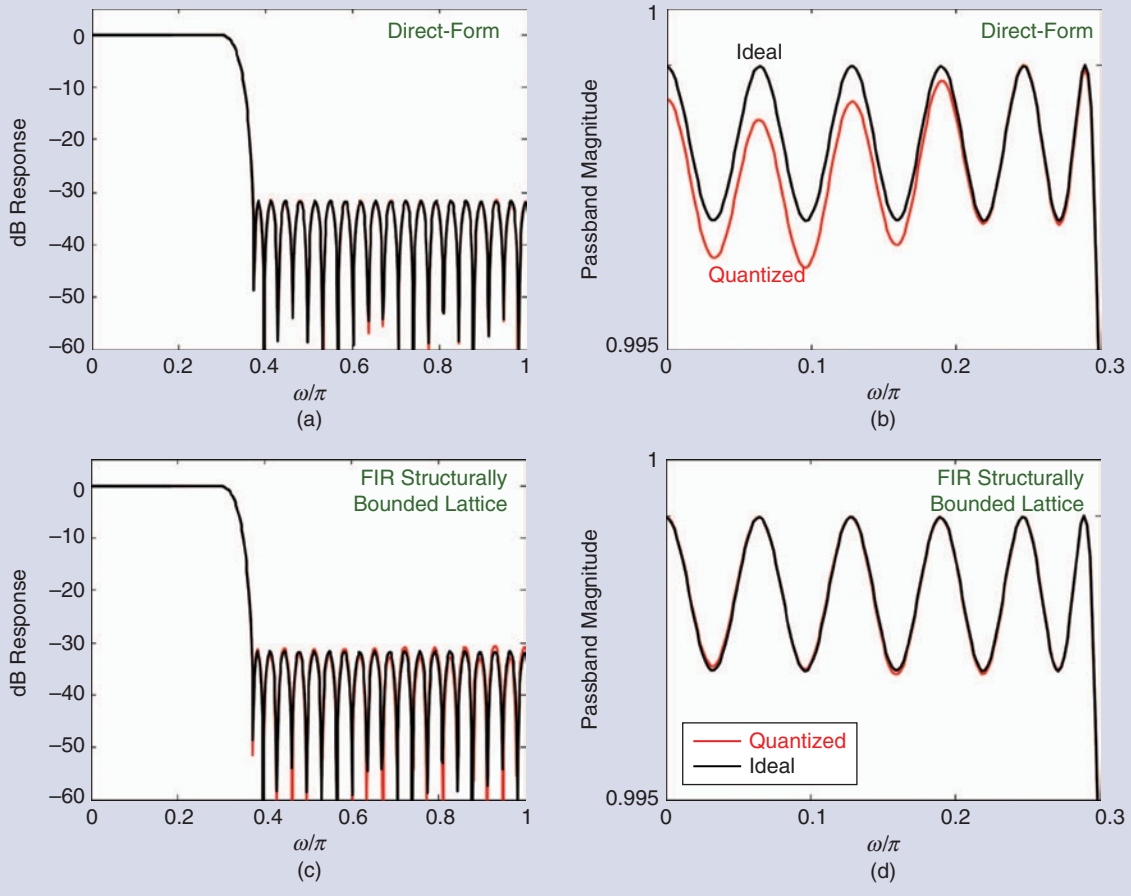


Figure 15. Responses of the direct-form structure and the FIR structurally passive lattice [78] under quantization. A 60th order FIR filter $H_0(z)$ is simulated, and coefficients are quantized to 8 bits. The responses of quantized structures are shown in red, and responses of unquantized structures are in black. Notice the low passband sensitivity of the structurally passive FIR lattice.

In fact, these power complementary FIR lattices have also inspired the theory of multirate filter banks with perfect reconstruction, leading to a whole generation of filter bank structures with orthogonality properties.

We conclude by mentioning some generalizations. If $\{H_0(z), H_1(z), \ldots, H_{M-1}(z)\}$ are causal real coefficient FIR filters with power complementary property, that is, $\sum_k |H_k(e^{j\omega})|^2 = 1$, then there exists a cascaded lattice structure similar in principle to Fig. 14(a), and can be implemented with planar rotations as the only computational units. For details please see [78]. Such structures are useful in the implementation of power complementary filter banks. In fact, these power complementary FIR lattices have also inspired the theory of multirate filter banks with perfect reconstruction, leading to a whole generation of filter bank structures with orthogonality properties. Details can be found in [1], [41], [46], [47], [65], [82], [84]–[88]. Such filter banks retain the perfect-reconstruction property in spite of coefficient quantization, and this can be exploited in the design of the filter responses under quantized conditions [36]. In addition to their applications in signal compression and digital communications, orthonormal filter banks have a role in the construction of orthonormal wavelets [11], [14], [66], [88], [91].

C. The FIRBR Structure

We now present an example of a structurally passive FIR system called the **FIRBR** structure [74]. It is one of the simplest ways to achieve structural passivity – the only background required is a first course in digital signal processing. The method only works for Type 1 linear phase FIR filters [54] with equiripple passbands. Such a filter has transfer function of the form $H(z) = \sum_{n=0}^{N} h(n) z^{-n}$ and satisfies the following properties:

1) N is even,
2) $h(n)$ is real, and
3) $h(n)$ is symmetric, that is $h(n) = h(N-n)$.

So the frequency response has the form

$$H(e^{j\omega}) = e^{-j\omega N/2} H_R(e^{j\omega}) \tag{22}$$

where $H_R(e^{j\omega})$ is called the zero-phase part. It is real, with $H_R(e^{j\omega}) \geq 0$ in the passband. Figure 16(a) shows a plot of the zero-phase part $H_R(e^{j\omega})$ for a lowpass filter. The equiripple property ensures in particular that all the peaks in the passband are equal to unity.

We now show how to implement such a filter in a structurally passive manner. Define the companion filter

$$G(z) = z^{-N/2} - H(z) \tag{23}$$

so that

$$G(e^{j\omega}) = e^{-j\omega N/2} \underbrace{(1 - H_R(e^{j\omega}))}_{G_R(e^{j\omega})} \tag{24}$$

Clearly this is a Type 1 linear phase highpass filter with zero-phase response $G_R(e^{j\omega})$ as shown in the figure. Furthermore, its response satisfies $G_R(e^{j\omega}) \geq 0$ for all ω. In fact at the passband peak frequencies of $H(z)$ where $H_R(e^{j\omega}) = 1$ and its derivative is zero, we have $G_R(e^{j\omega}) = 0$ and these are guaranteed to be *double zeros* of $G(z)$. Therefore $G(z)$ can be factorized into the form

$$G(z) = \underbrace{\prod_{k=1}^{M} (1 - 2z^{-1}\cos\omega_k + z^{-2})^2}_{G_1(z)} G_2(z) \tag{25}$$

where $G_1(z)$ represents all the double zeros on the unit circle and $G_2(z)$ represents all zeros which are not on the unit circle. So we can implement the original lowpass filter $H(z) = z^{-N/2} - G(z)$ using the structure shown in Fig. 16(b) where $G(z)$ is implemented in the factored form (25).

Now consider the effect of quantization. $G_1(z)$ is implemented in the factored form (25) where the multipliers are

$$m_k = 2\cos\omega_k \tag{26}$$

So if these multipliers are perturbed slightly, the zeros of $G_1(z)$ remain on the unit circle and they continue to be double zeros (as long as the quantized m_k satisfies $|m_k| \leq 2$). So $G_R(e^{j\omega}) \geq 0$ which shows that $H_R(e^{j\omega}) \leq 1$.

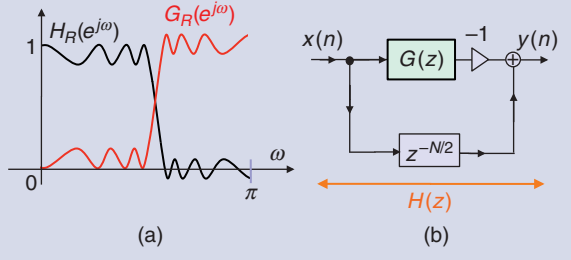


Figure 16. (a) The relation between the responses of $H(z)$ and $G(z)$ where $H(z)$ is Type-1 linear phase FIR, and $G(z) = z^{-N/2} - H(z)$. Here $H_R(e^{j\omega})$ and $G_R(e^{j\omega})$ are the zero-phase responses of $H(z)$ and $G(z)$ as defined in Eqs. (22) and (24). (b) An implementation of $H(z)$. If $G(z)$ is implemented in the factored form (25), this implementation of $H(z)$ is structurally passive. This is called the FIRBR implementation, and enjoys low passband sensitivity.

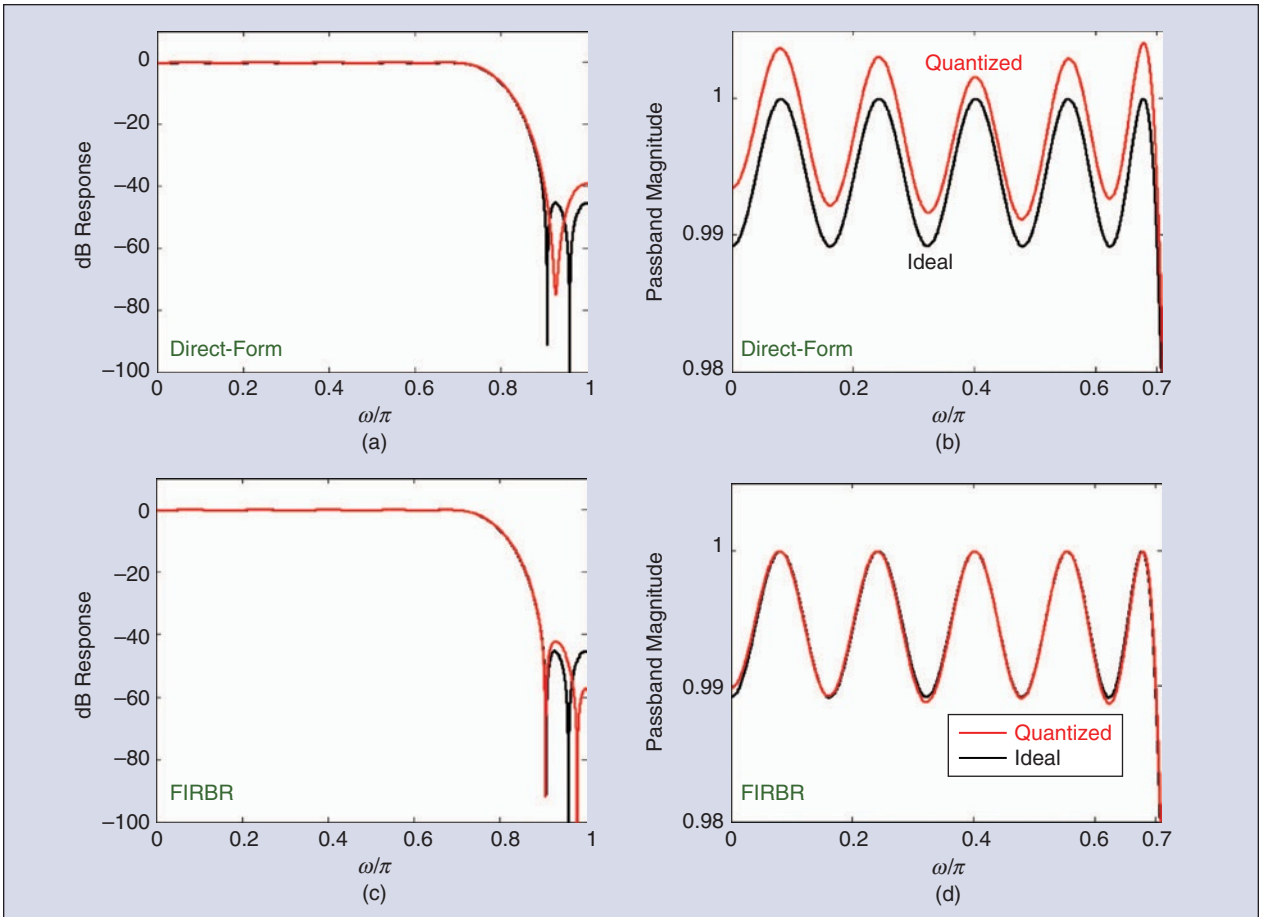


Figure 17. Responses of the direct-form structure and the FIRBR structure [74] under quantization. A 24th order linear phase FIR filter $H(z)$ is simulated, and coefficients are quantized to 7 bits. The responses of quantized structures are shown in red, and responses of unquantized structures are in black. Notice the low passband sensitivity of the FIRBR structure, induced by structural passivity.

Thus the passband response of $H(z)$ *remains bounded by unity*.[1] Fig. 16(b) is therefore a structurally bounded implementation as long as $G(z)$ is implemented in factored form (25). The structure therefore enjoys low passband sensitivity.

To demonstrate the low sensitivity, we consider a 24th order linear phase lowpass equiripple filter $H(z)$ designed using the McClellan-Parks algorithm [54]. We implement this using Fig. 16(b), with $G(z)$ implemented in factored form (25). We compare the resulting frequency response with those of the direct-form structure, with multipliers quantized to 7 bits in both structures. Fig. 17 shows the filter magnitude responses for these implementations. The responses of quantized structures are shown in red, and responses of unquantized structures are in black. For both structures, the dB plot of the entire response is shown, and the details of the passband region is shown separately. While the structures have comparable performances in the stopband, the passband response of the quantized direct-form deviates significantly from the ideal. In contrast, the quantized response of the structurally passive implementation (FIRBR structure of Fig. 16(b)) is nearly perfect in the passband as well, demonstrating very low passband sensitivity.

[1]Notice that $G_2(z)$ is itself a Type 1 linear phase filter, and has zeros in reciprocal conjugate pairs $\{z_k, 1/z_k^*\}$. When the coefficients of $G_2(z)$ are quantized, these zeros continue to remain inside and outside the unit circle, with reciprocal conjugate symmetry.

VI. Concluding Remarks

The world of circuit theory has been home to many legends in the last hundred years who gave a rock solid foundation to the field. Prof. Fettweis was one such giant who was a legend even during his life time. His contributions spanned a much wider area than we have discussed in this limited space. In this article we focussed only on digital filter structures with low passband sensitivity. Even in the area of wave digital filters, low sensitivity is only one of the many aspects addressed by Prof. Fettweis. His contributions to other aspects of robustness such as freedom from limit cycles are addressed in other articles in this issue.

P. P. Vaidyanathan (S'80–M'83–SM'88–F'91) is the Kiyo and Eiko Tomiyasu Professor of Electrical Engineering at the California Institute of Technology, where he has been on the faculty since 1983. He has authored over 500 papers and four books in the signal processing area. He is a Fellow of the IEEE, and a recipient of the IEEE CAS Society Golden Jubilee Medal, and the F. E. Terman Award of the American Society for Engineering Education. He has received multiple awards for excellence in teaching at the California Institute of Technology, including the Northrop Grumman prize for excellence in teaching. In 2016 he received the IEEE Gustav Robert Kirchhoff Award for "fundamental contributions to digital signal processing." He is a recipient of the IEEE Signal Processing Society Technical Achievement Award (2002), Education Award (2012), and Society Award (2016).

Sanjit K. Mitra (S'59–M'63–SM'69–F'74) is a Research Professor in the Department of Electrical & Computer Engineering, University of California, Santa Barbara and Professor Emeritus, Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles. Dr. Mitra has served IEEE in various capacities including service as the President of the IEEE Circuits & Systems Society in 1986. He is a member of the U.S. National Academy of Engineering, a member of the Norwegian Academy of Technological Sciences, an Academician of the Academy of Finland, a foreign member of the Finnish Academy of Sciences and Arts, a foreign member of the Croatian Academy of Sciences and Arts, Croatian Academy of Engineering, and the Academy of Engineering, Mexico, and a Foreign Fellow of the National Academy of Sciences, India and the Indian National Academy of Engineering. Dr. Mitra is a Life Fellow of the IEEE.

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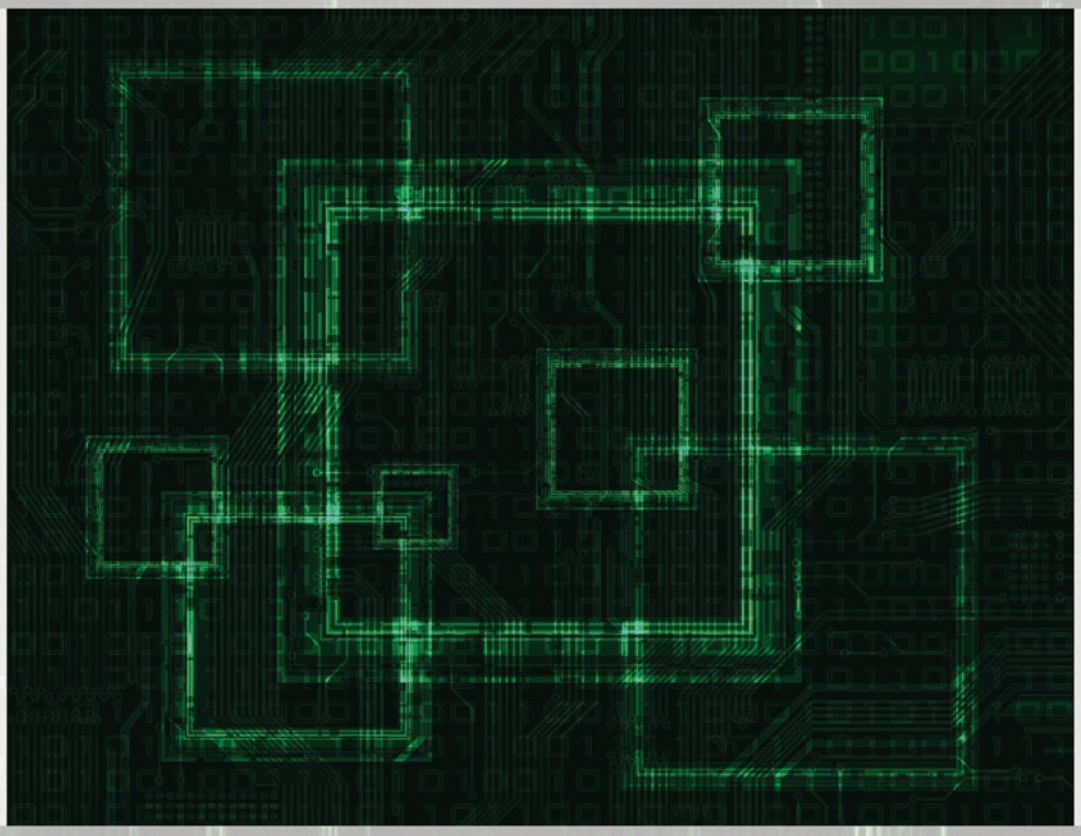

Symmetry Incorporated Cost-Effective Architectures for Two-Dimensional Digital Filters

Lan-Da Van, *Senior Member, IEEE*, I-Hung Khoo, *Member, IEEE*,
Pei-Yu Chen, Haranatha (Hari) C. Reddy, *Life Fellow, IEEE*

Abstract

Professor Fettweis as far back as 1977 published a paper generalizing McClellan transformation to obtain circular symmetry in 2-D and spherical, hyper-spherical symmetries in multidimensional digital filters [1]. This survey paper presents state-of-the-art two-dimensional (2-D) VLSI digital filter architectures possessing various symmetries in the filter magnitude response. Preceding the symmetry structures, a generalized formulation is given that allows the derivation of various new 2-D VLSI filter structures of any order without global broadcast. Following this, two types (namely, Type 1 [20] and Type 3 [21], [25], [26]) of cost-effective 2-D magnitude symmetry filter architectures possessing diagonal, four-fold rotational, quadrantal, and octagonal symmetries with reduced number of multipliers are given. By combining the identities of the Types-1 and 3 symmetry filter structures, multimode 2-D symmetry filters which enable the above four symmetry modes are discussed. The Type-1 and Type-3 multimode filters can result in a 65.3% cost reduction in terms of number of multipliers compared with the sum of the multipliers of the four individual Type-1 symmetry filter structures studied in this paper. Furthermore, Type-3 has shorter critical path than Type-1 multimode filter. The paper is concluded with the presentation of a 2-D filter design example and a corresponding structure.

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I. Introduction

Since 1970s, the theory and design of two-dimensional (2-D) digital filters [1]–[15] has attracted much attention in the digital signal processing field. Although 2-D digital filters can be implemented on a general-purpose processor for various DSP applications, the requirements of high-throughput and low-power issues result in dedicated computing architectures. Several conventional VLSI architectures for 2-D filters have been studied in [11]–[13], and an existing application specific integrated circuit (ASIC) approach has been applied to the design of beam filters [14], [15], and 2-D symmetry filters [16]–[26]. In his paper [1], Fettweis discussed the need for circular symmetry in the magnitude response of 2-D filters. Since circular symmetry cannot be achieved exactly by a rational 2-D transfer function, researchers have focused on achieving symmetries that can approximate the circular symmetry. Therefore, the quadrantal, diagonal, four-fold rotational and octagonal symmetries [8], [9] that help achieve circular symmetry were extensively studied. These symmetries are also needed not only to approximate circular symmetry but also to design Fan, Cone and other filter specifications. The most notable summarization of the research on 2-D symmetry till mid-1980s was done by Swamy and Rajan [8]. Recently the authors have presented efficient 2-D digital filter architectures incorporating these magnitude symmetries. From BIBO stability point of view, incorporating quadrantal, four-fold rotational and octagonal symmetries require separable denominators in the variables. This is considered in the architectures studied by the authors. The significant feature of the filters studied in [18], [19] is that they exhibit the denominator separability as a filter structural property. This means that the separability of the denominator is maintained independent of the choice of multiplier values. This important property is essential for the design of the multimode symmetry filter discussed in this review paper.

It is well-known that the presence of symmetry in the frequency responses of 2-D filters can be used to reduce the number of multipliers [8]–[10]. Consequently, several potential 2-D filter architectures that make use of filter symmetries have been explored [16]–[26]. In this paper, six cost-effective symmetry filter architectures (i.e., four Type-1 and two Type-3) are reviewed and discussed. They possess diagonal, four-fold rotational, quadrantal, and octagonal symmetries, and require fewer multipliers compared to structures that do not use symmetry. Further, to integrate the support of multiple symmetry functions, two cost-effective Type-1 and Type-3 multimode 2-D filter designs with four symmetries mentioned above is proposed. Type 2 architectures [20] are not reviewed due to space limitation. This paper is organized as follows: Section II describes the various symmetries and their constraints on the coefficients of the 2-D polynomial. Section III discusses the general formulation of 2-D filter architectures. Section IV presents different VLSI suitable filter architectures with symmetry, that require fewer number of multipliers. In Section V, two cost-effective multimode filter architectures with four symmetries are discussed. The error analyses of filter structures are discussed in Section VI. The cost in terms of number of multipliers and adders of the reviewed symmetry filter structures and the multimode filter architecture are profiled and evaluated in Section VII. A filter design example is given in Section VIII. The summary of the results are given in Section IX.

II. Various Symmetries and Constraints on the Coefficients of 2-D Polynomials

A real general 2-D z-domain IIR transfer function can be represented as in (1), where a_{ij} and b_{ij} are real coefficients and $b_{00} = 0$, $N_1 \times N_2$ is the order of the filter, and X and Y are respectively the input and output of the filter. The equation can also represent an FIR transfer function if we set $b_{ij} = 0$ for all i and j.

$$H(z_1, z_2) = \frac{Y(z_1, z_2)}{X(z_1, z_2)} = \frac{\sum_{i=0}^{N_1}\sum_{j=0}^{N_2} a_{ij} z_1^{-i} z_2^{-j}}{1 - \sum_{i=0}^{N_1}\sum_{j=0}^{N_2} b_{ij} z_1^{-i} z_2^{-j}} = \frac{P(z_1, z_2)}{Q(z_1, z_2)} \tag{1}$$

The usefulness of symmetry relations in the design of 2-D filters have been studied extensively [1], [5]–[10]. The symmetry present in the frequency response induces a relation among the filter coefficients and multipliers in the filter structures. This reduces the number of design parameters in an optimization scheme, as well as the number of multipliers in an implementation architecture. There are many possible types of symmetries in the magnitude response such as quadrantal, diagonal, four-fold rotational, and octagonal symmetries.

The frequency response is evaluated on the distinguished boundary of the unit bi-disk, $z_i = e^{j\theta_i}, i = 1, 2$, as shown in Fig. 1. If $P(z_1, z_2)$ is a 2-D z-domain real

L. D. Van, H.C. Reddy, P. Y. Chen are with the Dept. of Computer Science, National Chiao Tung University, Hsinchu, 300, Taiwan, R.O.C. I. H. Khoo and H. C. Reddy* are with Dept. of Electrical Engineering, California State University Long Beach, Long Beach, CA, U.S.A.* *This work was supported in part by the MOST 106-2221-E-009-028-MY3, MOST 106-2218-E-009-029 and MOST 107-2634-F-009-010.*

The existence of symmetry in $F(\theta_1, \theta_2)$ implies that the value of the function at (θ_1, θ_2) on the distinguished boundary is related to the value of the function at $(\theta_{1T}, \theta_{2T})$ where $(\theta_{1T}, \theta_{2T})$ is obtained by some operation on (θ_1, θ_2).

polynomial, its frequency response is given by $P(e^{j\theta_1}, e^{j\theta_2})$. The magnitude squared function of the frequency response is given by:

$$\begin{aligned} F(\theta_1, \theta_2) &= |P(e^{j\theta_1}, e^{j\theta_2})|^2 \\ &= P(e^{j\theta_1}, e^{j\theta_2}) \cdot P(e^{-j\theta_1}, e^{-j\theta_2}) \\ &= P(z_1, z_2) \cdot P(z_1^{-1}, z_2^{-1})\big|_{z_i = e^{j\theta_i},\, i=1,2} \end{aligned} \tag{2}$$

It can be seen from (2) that the Centro-Symmetric property, i.e., $F(\theta_1, \theta_2) = F(-\theta_1, -\theta_2)$ is always satisfied. The existence of symmetry in $F(\theta_1, \theta_2)$ implies that the value of the function at (θ_1, θ_2) on the distinguished boundary is related to the value of the function at $(\theta_{1T}, \theta_{2T})$ where $(\theta_{1T}, \theta_{2T})$ is obtained by some operation on (θ_1, θ_2) as shown in Figure 2. Also, for our discussion, we assume that the value of the magnitude function is unchanged, i.e., $F(\theta_1, \theta_2) = F(\theta_{1T}, \theta_{2T})$. A more detailed discussion of this can be found in [8]–[10]. Now consider the following symmetries:

Quadrantal Symmetry

If the magnitude squared function possesses quadrantal symmetry, then

$$F(\theta_1, \theta_2) = F(-\theta_1, \theta_2) = F(\theta_1, -\theta_2) = F(-\theta_1, -\theta_2), \forall (\theta_1, \theta_2) \tag{3}$$

Expressing (3) in terms of the polynomial yields:

$$\begin{aligned} &P(z_1, z_2) \cdot P(z_1^{-1}, z_2^{-1}) \cdot z_1^{-N_1} \cdot z_2^{-N_2} \\ &= P(z_1^{-1}, z_2) \cdot P(z_1, z_2^{-1}) \cdot z_1^{-N_1} \cdot z_2^{-N_2} \end{aligned} \tag{4}$$

Note that the multiplication by $z_1^{-N_1} \cdot z_2^{-N_2}$ is needed so that both sides of the equation remain a polynomial in negative powers of z. Applying the unique factorization property of 2-variable polynomials [8] to (4), it can be seen that the factors of $P(z_1, z_2)$ should satisfy one of the following two conditions:

i) $P(z_1, z_2) = k_1 \cdot P(z_1^{-1}, z_2) \cdot z_1^{-N_1}$ where k_1 is a real constant.

ii) $P(z_1, z_2) = k_2 \cdot P(z_1, z_2^{-1}) \cdot z_2^{-N_2}$ where k_2 is a real constant.

Each of the above conditions will provide a constraint on the polynomial for it to possess quadrantal symmetry in its magnitude response.

Substituting $P(z_1, z_2) = \Sigma_{i=0}^{N_1} \Sigma_{j=0}^{N_2} a_{ij} \cdot z_1^{-i} \cdot z_2^{-j}$ into condition (i) above and assuming $k_1 = 1$, we get:

$$\sum_{i=0}^{N_1} \sum_{j=0}^{N_2} a_{ij} \cdot z_1^{-i} \cdot z_2^{-j} = \sum_{i=0}^{N_1} \sum_{j=0}^{N_2} a_{ij} \cdot z_1^{i-N_1} \cdot z_2^{-j} \tag{5}$$

Applying a change of variable $i' = N_1 - i$ to (5), we obtain:

$$\sum_{i=0}^{N_1} \sum_{j=0}^{N_2} a_{ij} \cdot z_1^{-i} \cdot z_2^{-j} = \sum_{i'=0}^{N_1} \sum_{j=0}^{N_2} a_{N_1-i',j} \cdot z_1^{-i'} \cdot z_2^{-j} \tag{6}$$

So, the coefficient constraint $a_{ij} = a_{N_1-i,j}$ will ensure that the polynomial $P(z_1, z_2)$ possesses quadrantal symmetry in its magnitude response. The same steps can be applied to condition (ii) above to obtain another coefficient constraint:

$$a_{ij} = a_{i,N_2-j} \tag{7}$$

These coefficient constraints can be applied to the transfer function of an FIR filter to ensure quadrantal symmetry. For an IIR filter, the constraint can be applied to the numerator polynomial. To satisfy the coefficient condition $a_{ij} = a_{N_1-i,j}$ with the requirement of BIBO stability, the denominator $Q(z_1, z_2)$ must be chosen as a variable separable one [8], i.e., as $Q(z_1, z_2) = Q_A(z_1) \cdot Q_B(z_2)$. It is easy to see that $Q_A(z_1)$ satisfies $a_{ij} = a_{i,N_2-j}$ and $Q_B(z_2)$ satisfies $a_{ij} = a_{N_1-i,j}$, so their product possesses quadrantal symmetry. In addition, because the denominator is separable, it is easy to check the stability of the filter structure.

Following the above, the coefficient conditions for diagonal and four-fold rotational symmetries can be obtained using the appropriate conditions on the magnitude squared function.

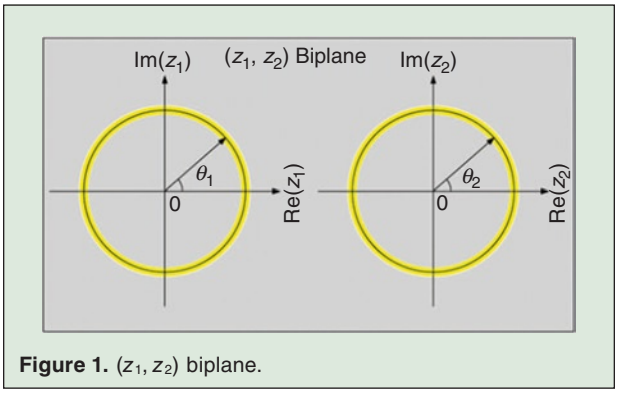


Figure 1. (z_1, z_2) biplane.

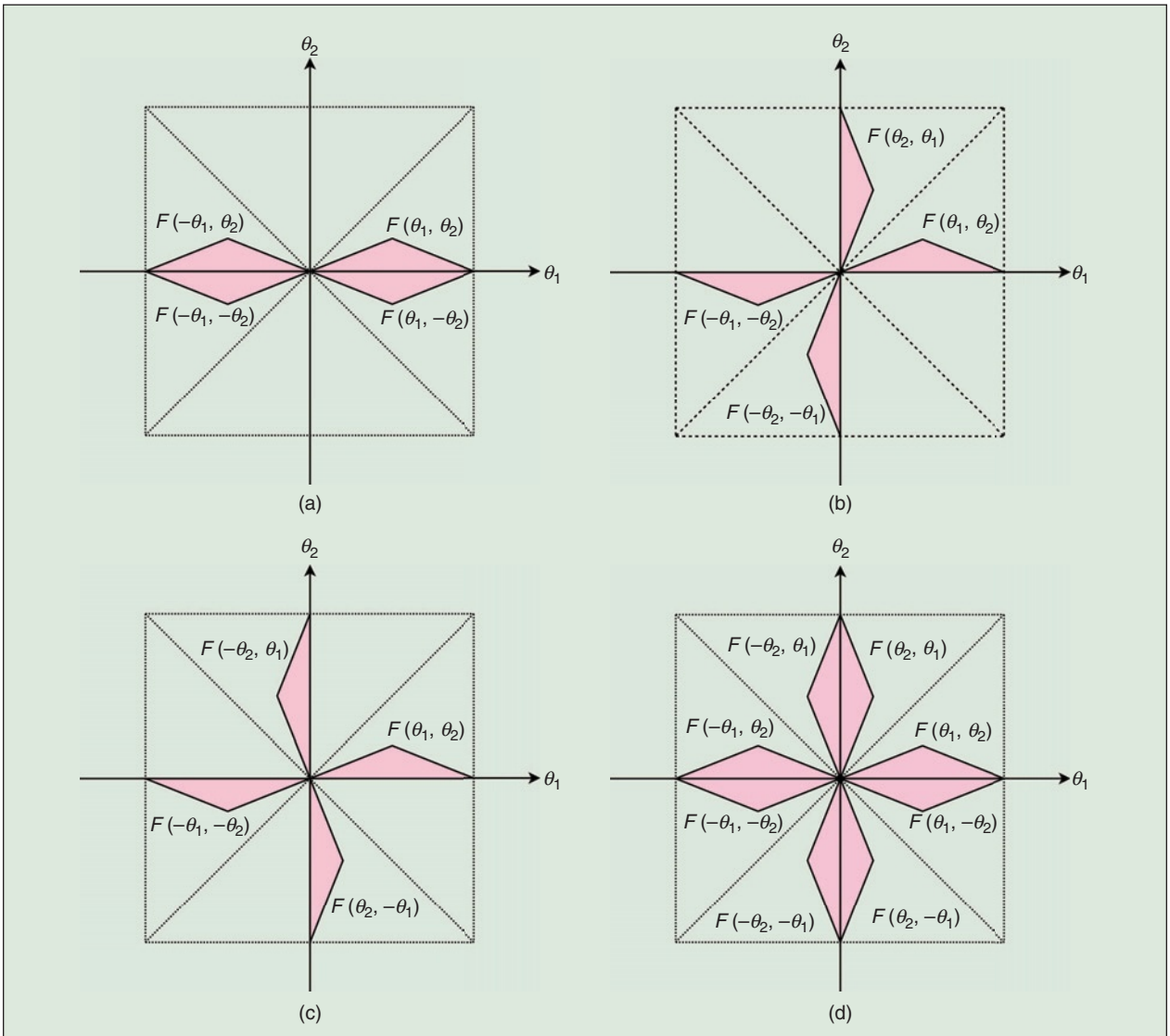


Figure 2. (a) Quadrantal Symmetry (b) Diagonal Symmetry (c) Rotational Symmetry (d) Octagonal Symmetry.

Diagonal Symmetry

The constraint on the magnitude response for the diagonal symmetry is:

$$F(\theta_1, \theta_2) = F(\theta_2, \theta_1) = F(-\theta_1, -\theta_2) = F(-\theta_2, -\theta_1) \quad (8)$$

The coefficient conditions resulting from the above by following the steps described for quadrantal symmetry are:

$$N_1 = N_2 = N$$
$$\text{and} \quad a_{ij} = a_{ji} \quad \text{for} \quad 0 \le i, j \le N \quad (9)$$
$$\text{or} \quad a_{ij} = a_{N-j,N-i} \quad \text{for} \quad 0 \le i, j \le N \quad (10)$$

Similar conditions should be satisfied by the denominator $Q(z_1, z_2)$ in addition to satisfying the BIBO stability conditions.

Four-Fold Rotational Symmetry

The magnitude response condition for this symmetry is:

$$F(\theta_1, \theta_2) = F(-\theta_2, \theta_1) = F(-\theta_1, -\theta_2) = F(\theta_2, -\theta_1) \quad (11)$$

The coefficient conditions resulting from the above will be:

$$N_1 = N_2 = N$$
$$\text{and} \quad a_{ij} = a_{N-j,i} \quad \text{for } 0 \le i, j \le N \quad (12)$$
$$\text{or} \quad a_{ij} = a_{j,N-i} \quad \text{for} \quad 0 \le i, j \le N \quad (13)$$

The denominator $Q(z_1, z_2)$ of a BIBO stable filter with four-fold rotational symmetry should be of the form $Q(z_1, z_2) = Q_A(z_1) \cdot Q_A(z_2)$.

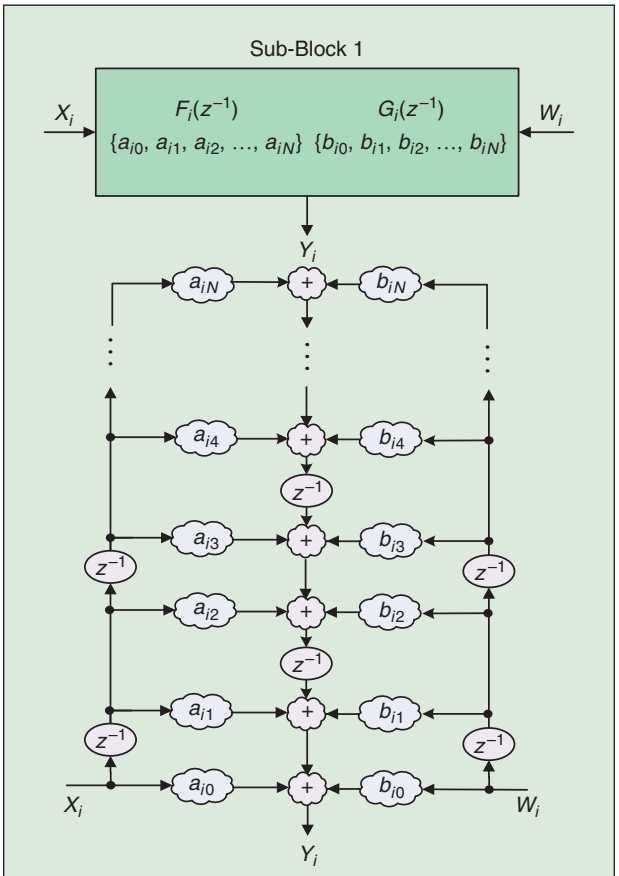


Figure 3. Sub-block #1 (2-inputs-1-outputs, direct-form).

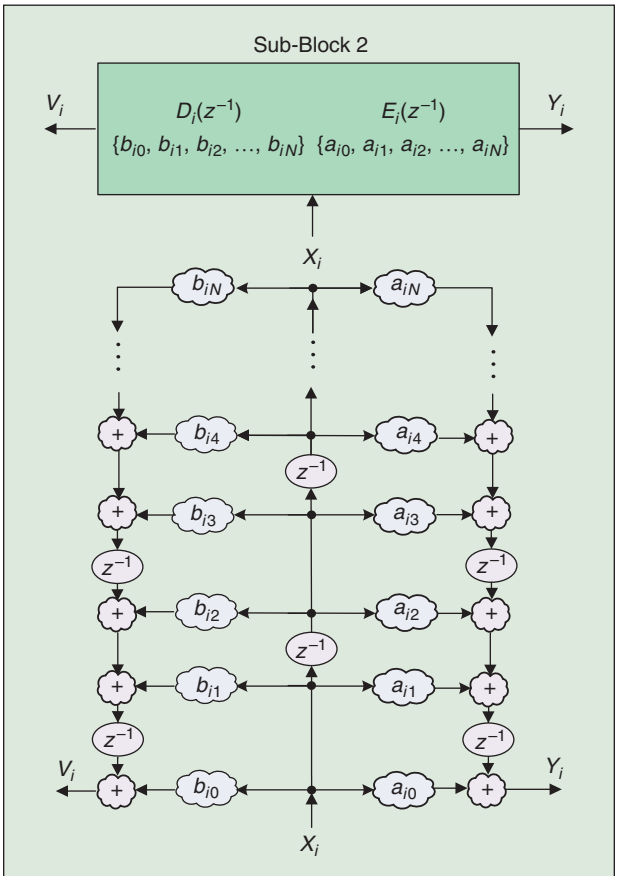


Figure 4. Sub-block #2 (1-input-2-outputs, direct-form).

If any two of the above three symmetries are satisfied, the resulting symmetry will be an octagonal symmetry.

The above coefficient conditions on 2-D filter transfer function form the basis for deriving various symmetry incorporated architectures with reduced number of multipliers.

The sample sectors for various symmetries are illustrated in (θ_1, θ_2)-plane in Fig. 2. These figures show the shaded region where $F(\theta_1, \theta_2) = F(\theta_{1T}, \theta_{2T})$.

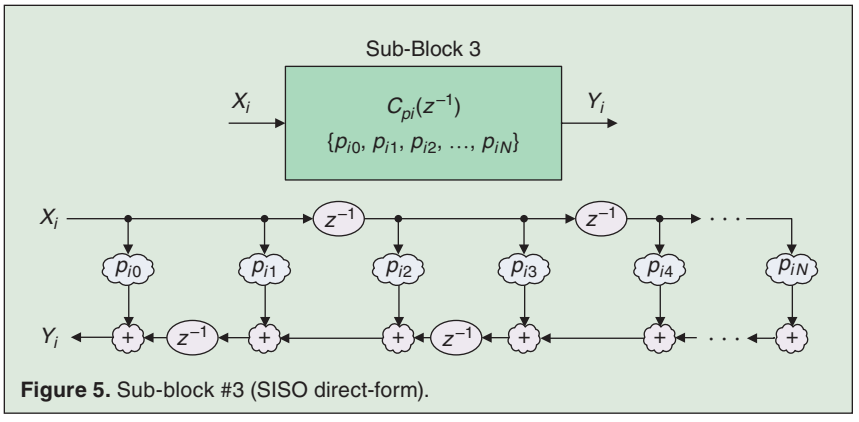


Figure 5. Sub-block #3 (SISO direct-form).

III. Generalized Formulation of 2-D Filter Architectures without Global Broadcast

The transfer function in (1) can also be expressed as:

$$H(z_1, z_2) = \frac{\sum_{i=0}^{N_1} F_i(z_2^{-1}) \cdot z_1^{-i}}{1 - \sum_{i=0}^{N_1} G_i(z_2^{-1}) \cdot z_1^{-i}} \qquad (14)$$

where $F_i(z_2^{-1}) = \Sigma_{j=0}^{N_2} a_{ij} z_2^{-j}$ and $G_i(z_2^{-1}) = \Sigma_{j=0}^{N_2} b_{ij} z_2^{-j}$ with $b_{00} = 0$ are 1-D FIR functions in z_2 variable only. These 1-D functions can be realized by the sub-blocks in Figs. 3 to 5. These sub-blocks are then used in the filter frameworks to realize the overall 2-D transfer function in (14).

In our discussion, we assume that the filter is used to process a zero padded image of size $M_1 \times M_2$ and the pixel values in the image are fed to the filter in raster-scan mode, i.e. the input sequence is $x(0,0), x(0,1), \ldots,$

The critical period is the time required for the signal through the slowest (critical) path of the architecture and determines the highest possible clock speed of the architecture.

$x(0, M_2-1), x(1,0), x(1,1), \ldots$ etc. We can then replace z_2^{-1} by a single delay register z^{-1} (usually implemented by a D flip-flop). z_1^{-1} can be replaced by a shift register (SR) of length M_2, z^{-M_2} (using M_2-size D flip-flops), provided $M_2 > N_2$. Without loss of generality, we will assume $N_1 = N_2 = N$ in discussing the filters.

Filter Sub-blocks

The filter sub-blocks are formulated as general digital two-pair networks to realize 1-D FIR functions in z_2. Here, we assume $z^{-1} = z_2^{-1}$. Sub-block #1, shown in Fig. 3, has 2 inputs and 1 output, where the coefficient inside the cloud symbol denotes a multiplier. It is direct form, i.e. the multiplier values are the same as the polynomial coefficients. It realizes the following two FIR functions.

$$F_i(z^{-1}) = \frac{Y_i}{X_i}\bigg|_{W_i=0} = \sum_{j=0}^{N} a_{ij} z^{-j},$$
$$G_i(z^{-1}) = \frac{Y_i}{W_i}\bigg|_{X_i=0} = \sum_{j=0}^{N} b_{ij} z^{-j} \qquad (15)$$

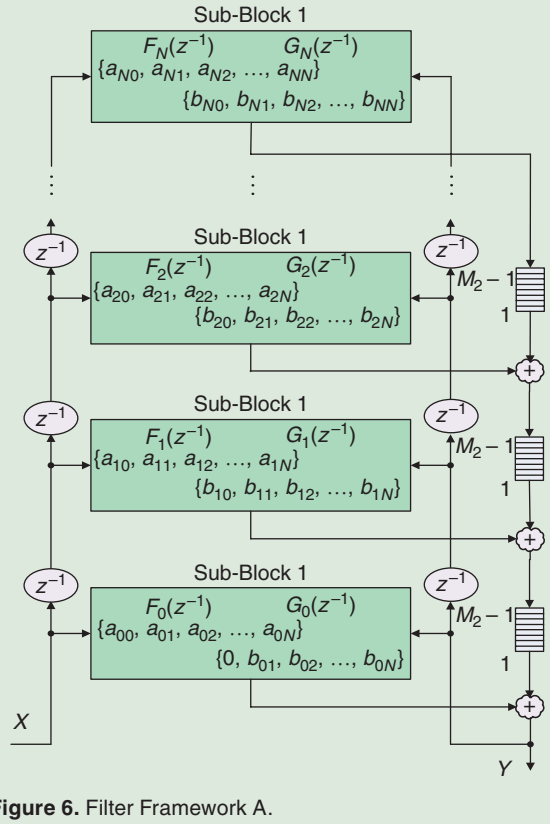


Figure 6. Filter Framework A.

Note that the special arrangement of the delays is to eliminate global broadcast of the signals, X_i and W_i, and to control the critical period. The critical period is the time required for the signal through the slowest (critical) path of the structure and determines the highest possible clock speed of the structure. A different filter sub-block (sub-block#2) as shown in Fig. 4 can be obtained by taking the transpose of filter sub-block#1, where $E_i(z^{-1})$ and $D_i(z^{-1})$ are similarly defined as (15). The sub-block #3 in Fig. 5 has single input and single output (SISO) and realizes the FIR function:

$$C_{\rho i}(z^{-1}) = \frac{Y_i}{X_i} = \sum_{j=0}^{N} \rho_{ij} z^{-j}$$

Note that ρ_{ij} can represent either the numerator or denominator coefficient a_{ij} or b_{ij}.

Filter Frameworks

The sub-blocks are used in the filter frameworks to realize the general 2-D z-domain transfer function in (1). Filter framework A shown in Fig. 6 uses the sub-block #1, where denotes the (M_2-1)-size D flip-flops/shift register. Notice that the shift registers are of length $M_2 - 1$ due to the additional delays added at the input and output branches to eliminate the global broadcast. It can be verified using Mason's gain formula that the structure with $z^{-1} = z_2^{-1}$ and SR $= z_1^{-1} z_2$ realizes the transfer function in (14). By taking the transpose of Framework A, a different filter framework can be obtained which utilizes sub-block#2 [23].

Structure Induced Separable Denominator Frameworks

By mixing the sub-blocks in specific ways, filter frameworks realizing transfer functions with separable denominator of the form in (16) can be obtained. The idea is to form two non-touching loops in different variables.

$$H(z_1, z_2) = \frac{Y(z_1, z_2)}{X(z_1, z_2)} = \frac{\sum_{i=0}^{N}\sum_{j=1}^{N} a_{ij} z_1^{-i} z_2^{-j}}{\left(1 - \sum_{i=1}^{N} b_{i0} z_1^{-i}\right) \cdot \left(1 - \sum_{j=1}^{N} b_{0j} z_2^{-j}\right)} \qquad (16)$$

Separable filter framework A1 is shown in Fig. 7. It is based on framework A. It uses sub-block #2 at the bottom while the rest are sub-block #1.

It realizes the transfer function in (17), with G_i's being constants.

$$\frac{Y}{X} = \frac{E_0(z_2) + \sum_{i=1}^{N} F_i(z_2) \cdot z_1^{-i}}{(1 - D_0(z_2)) \cdot \left(1 - \sum_{i=1}^{N} G_i(z_2) \cdot z_1^{-i}\right)} \tag{17}$$

By taking the transpose of filter frameworks A and A1, another set of frameworks can be obtained. Also, a different set of frameworks can be obtained using the sub-block #3. Due to lack of space, these frameworks are not shown here. A detailed discussion of sub-blocks, general frameworks, and separable denominator frameworks can be found in [23].

Explicit 2-D Filter Architectures

We will now use the sub-blocks in Figs. 3–5 and general frameworks to derive explicit architectures without global broadcast for separable denominator transfer functions. These are then used to incorporate symmetry. The separability is necessary to ensure the BIBO stability and at the same time to achieve quadrantal, four-fold rotational and octagonal symmetries in the filter magnitude response (note that separable denominator is not needed for the diagonal symmetry). In this section, we will focus on deriving structures for realizing (16). Using the sub-blocks in Figs. 3 and 4, the Type-1 separable denominator architecture in Fig. 8 can be obtained (for $N = 3$) [20]. The transfer function of the 2-D filter can be expressed as:

$$H(z_1, z_2) = \frac{Y_1(z_1, z_2)}{X(z_1, z_2)} \cdot \frac{Y(z_1, z_2)}{Y_1(z_1, z_2)} \tag{18}$$

where $$Y_1 = X + \sum_{i=1}^{N} b_{i0} z_1^{-i} Y_1 \tag{19}$$

Thus, $Y(z_1, z_2)/Y_1(z_1, z_2)$ can be generally represented as:

$$Y = \sum_{i=0}^{N} \sum_{j=0}^{N} a_{ij} z_1^{-i} z_2^{-j} Y_1 + \sum_{j=1}^{N} b_{0j} z_2^{-j} Y \tag{20}$$

It can be verified that the structures of Block 1 and Block 2 in Fig. 8 satisfy (19) and (20) respectively.

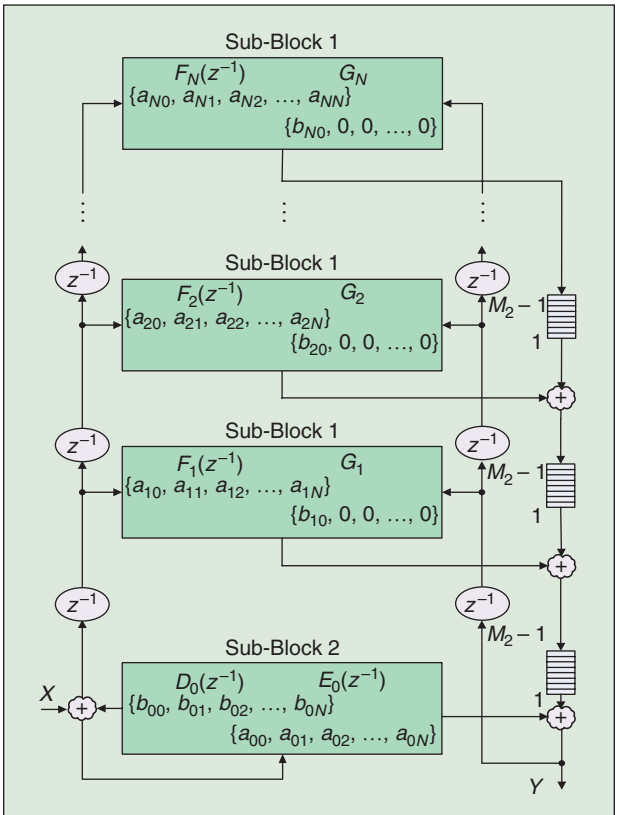


Figure 7. Filter Framework A1.

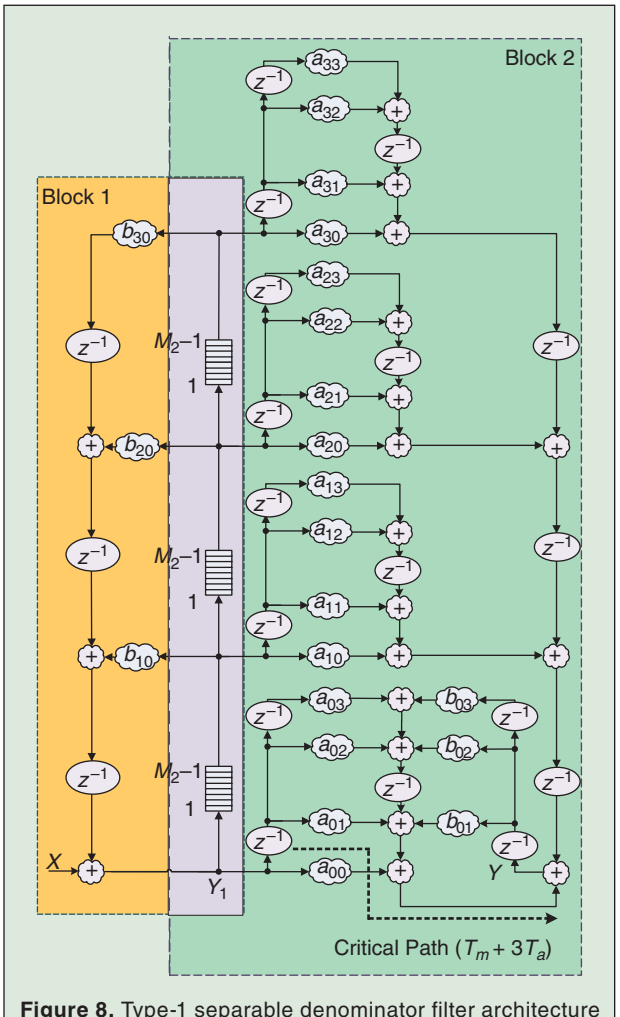


Figure 8. Type-1 separable denominator filter architecture ($N = 3$).

The Type-3 separable denominator architecture can be obtained (Fig. 9) using the sub-blocks in Figs. 3 and 5. Its transfer function can be rewritten as:

$$H(z_1, z_2) = \frac{Y(z_1, z_2)}{Y_3(z_1, z_2)} \cdot \frac{Y_3(z_1, z_2)}{X(z_1, z_2)} \tag{21}$$

$$\text{where } Y = Y_3 + \sum_{j=1}^{N} b_{0j} z_2^{-j} Y \tag{22}$$

Therefore, $Y_3(z_1, z_2)/X(z_1, z_2)$ can be expressed as:

$$Y_3 = \sum_{i=0}^{N} \sum_{j=0}^{N} a_{ij} z_1^{-i} z_2^{-j} X + \sum_{i=1}^{N} b_{i0} z_1^{-i} Y_3 \tag{23}$$

Using the tree method mentioned in [13] to arrange the adders, the critical periods for the Type 1 and Type 3 architectures are $T_m + 3T_a$ and $T_m + 2T_a$, respectively, where T_m and T_a denote the operation time required by one multiplier and one adder respectively. In the next section, we will focus on the Type-1 and Type-3 filter architectures with symmetry.

IV. Cost Effective 2-D Filter Architectures Incorporating Different Symmetries

The presence of symmetry in the 2-D frequency response induces certain relationship among the filter coefficients. This translates into reduced number of multipliers while implementing a 2-D digital filter architecture. In this section, we present six symmetry filter architectures with diagonal, four-fold rotational, quadrantal, and octagonal symmetries with separable denominators.

Diagonal Symmetry Filter Architectures

Applying the diagonal symmetry coefficient constraint (9) to the separable denominator transfer function in (16) implies that $a_{ij} = a_{ji}$ and $b_{k0} = b_{0k}$. Similarly, constraint

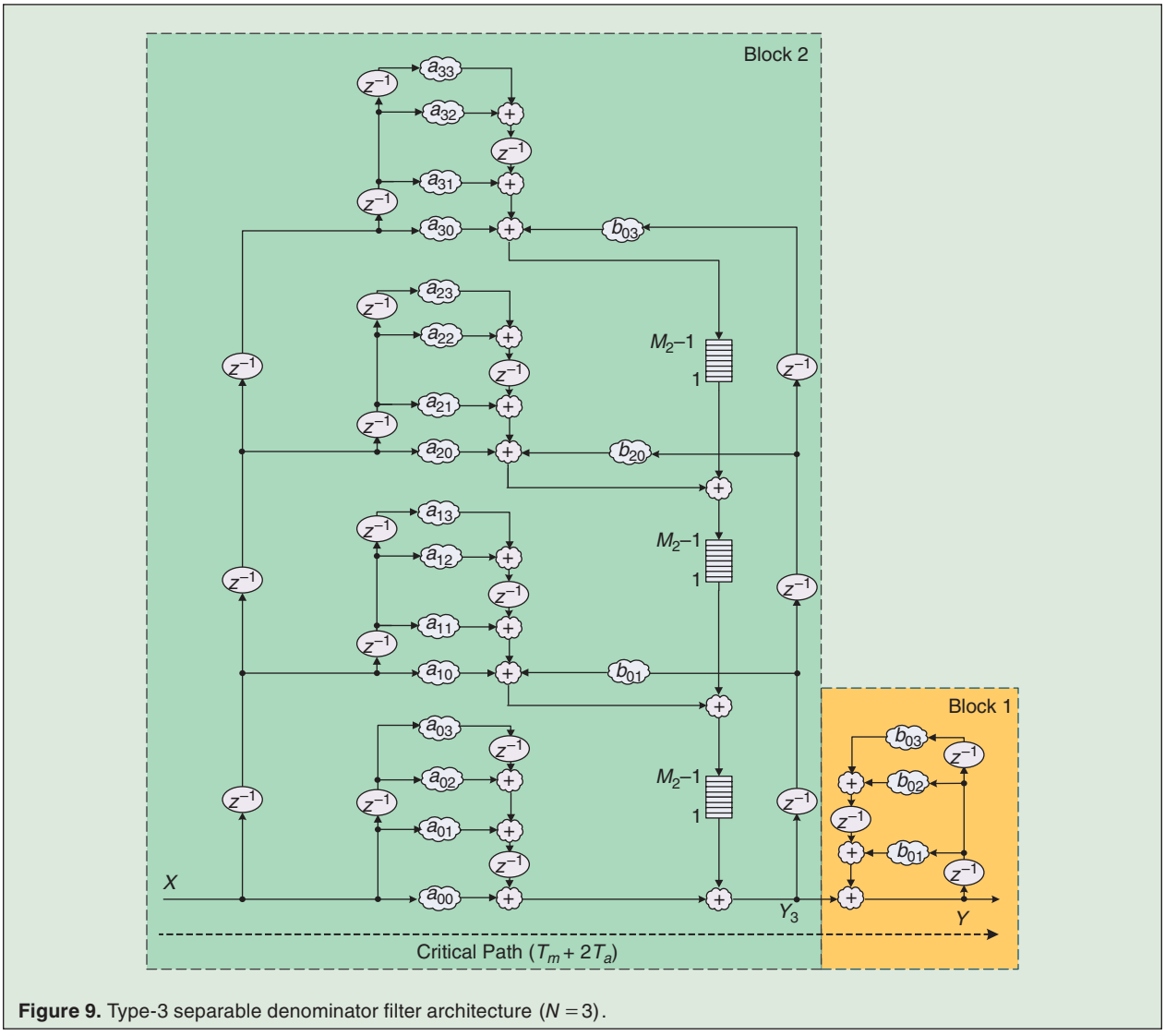


Figure 9. Type-3 separable denominator filter architecture ($N = 3$).

in (10) can be used to get different structures. Thus, for the Type-1 filter architecture, with Y_1 given in (19), the expression for the output Y in (20) can be recast as:

$$Y = \sum_{j=1}^{N} b_{0j} z_2^{-j} Y + \sum_{i=0}^{N} a_{ii} z_1^{-i} z_2^{-i} Y_1 + \sum_{i=0}^{N-1} \sum_{j=i+1}^{N} a_{ij} (z_1^{-i} z_2^{-j} + z_1^{-j} z_2^{-i}) Y_1 \quad (24)$$

Implementing (24) results in the Type-1 diagonal symmetry filter architecture of Fig. 10 [20]. Note that for diagonal symmetry, the denominator need not be separable, but they are used here for ease of the implementation of the multimode filter to be discussed in Section V.

In a similar way, one can obtain the Type 3 diagonal symmetry architecture shown in Fig. 11 [21]. Using the tree method to arrange the adders, the critical paths are shown in Figs. 10 & 11 for the two architectures. The critical periods are calculated as $T_m + 3T_a$ and $T_m + 2T_a$ respectively. Note that T_m and T_a denote the operation time required by the multiplier and adder respectively.

Four-fold Rotational Symmetry Filter Architectures

When the 2-D magnitude response of a filter possesses four-fold rotational symmetry, as per (13), the filter coefficients in (16) will satisfy the constraints: $a_{ij} = a_{j(N-i)}$ and $b_{k0} = b_{0k}$ for all i, j, k. So, for the Type-1 filter, the output Y in (20) for this symmetry can be expressed as:

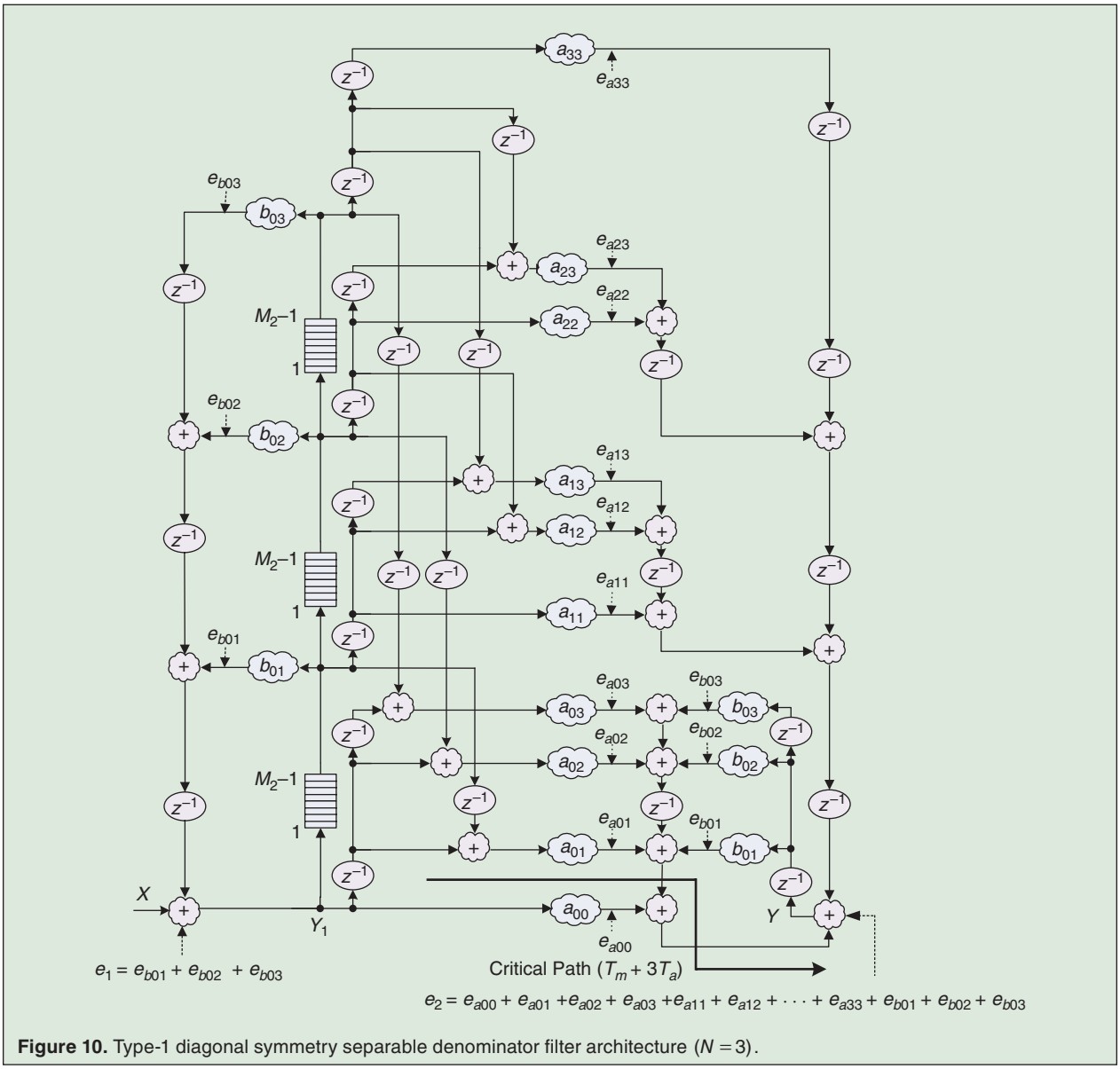


Figure 10. Type-1 diagonal symmetry separable denominator filter architecture ($N = 3$).

$$Y = \sum_{j=1}^{N} b_{0j} z_2^{-j} Y + v a_{uu} z_1^{-u} z_2^{-u} Y_1 + \sum_{i=0}^{u-v} \sum_{j=i}^{N-i-1} a_{ij} (z_1^{-i} z_2^{-j} + z_1^{-j} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-(N-j)} + z_1^{-(N-j)} z_2^{-i}) Y_1 \quad (25)$$

where $u = \lfloor N/2 \rfloor$, $v = (N+1)$ *mod 2, and* $\lfloor \cdot \rfloor$ denotes the largest integer that is smaller than or equal to $\cdot$. Figure 12 shows the Type-1 four-fold rotational symmetry filter architecture [20]. Following the above, the Type-3 four-fold rotational symmetry separable denominator filter

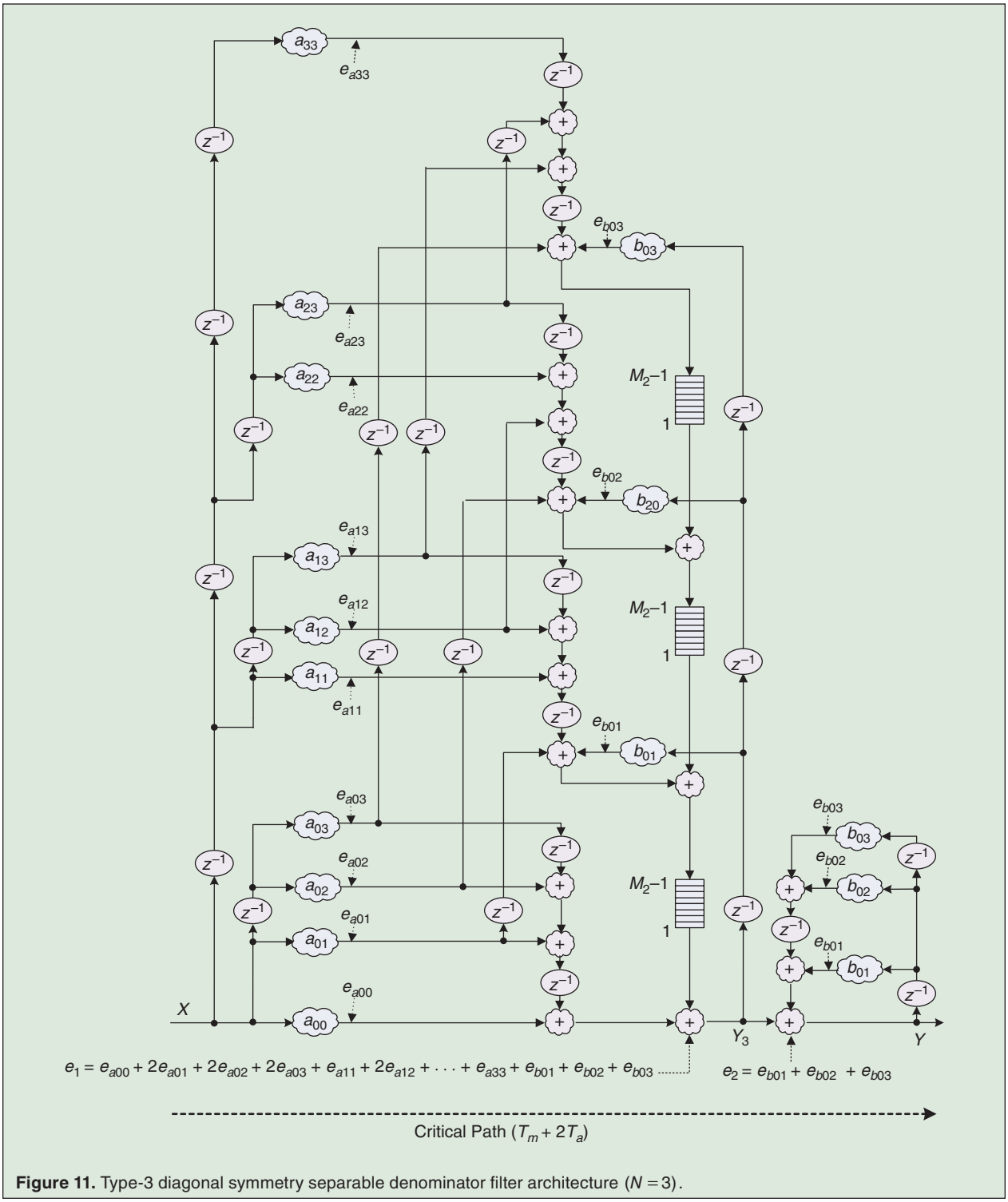


Figure 11. Type-3 diagonal symmetry separable denominator filter architecture ($N = 3$).

architecture can be obtained [21]. This structure is not shown here. Performing the critical path analysis on Fig. 12 yields the delay of $T_m + 3T_a$. For Type 3 structure, it will be $T_m + 2T_a$.

Quadrantal Symmetry Filter Architectures

When the 2-D magnitude response of a filter possesses quadrantal symmetry, as per (7) the filter coefficients in (16) will satisfy the constraints: $a_{ij} = a_{(N-i)j}$ and $b_{k0} = b_{0k}$ for all i, j, k. So, the output Y in (20) for the Type-1 filter becomes:

$$Y = \sum_{j=1}^{N} b_{0j} z_2^{-j} Y + v \cdot \sum_{j=0}^{N} a_{uj} (z_1^{-u} z_2^{-j}) Y_1 + \sum_{i=0}^{u-v} \sum_{j=0}^{N} a_{ij} (z_1^{-i} z_2^{-j} + z_1^{-(N-i)} z_2^{-j}) Y_1 \quad (26)$$

The Type-1 quadrantal symmetry filter architecture is given in Fig. 13 [20]. The Type 3 structure is shown in Fig. 14 [26].

Performing the critical path analysis using the tree method on Figs. 13 & 14 yield the delays of $T_m + 3T_a$ and $T_m + 2T_a$ respectively. The critical paths are indicated in the figures.

Octagonal Symmetry Filter Architectures

Octagonal symmetry is a combination of diagonal, four-fold rotational and quadrantal symmetries. Presence of any two of the three symmetries will guarantee the presence of octagonal symmetry in the 2-D magnitude response of the filter [8]–[10]. This results in the coefficient constraints, $a_{ij} = a_{ji} = a_{(N-i)j}$ and $b_{k0} = b_{0k}$

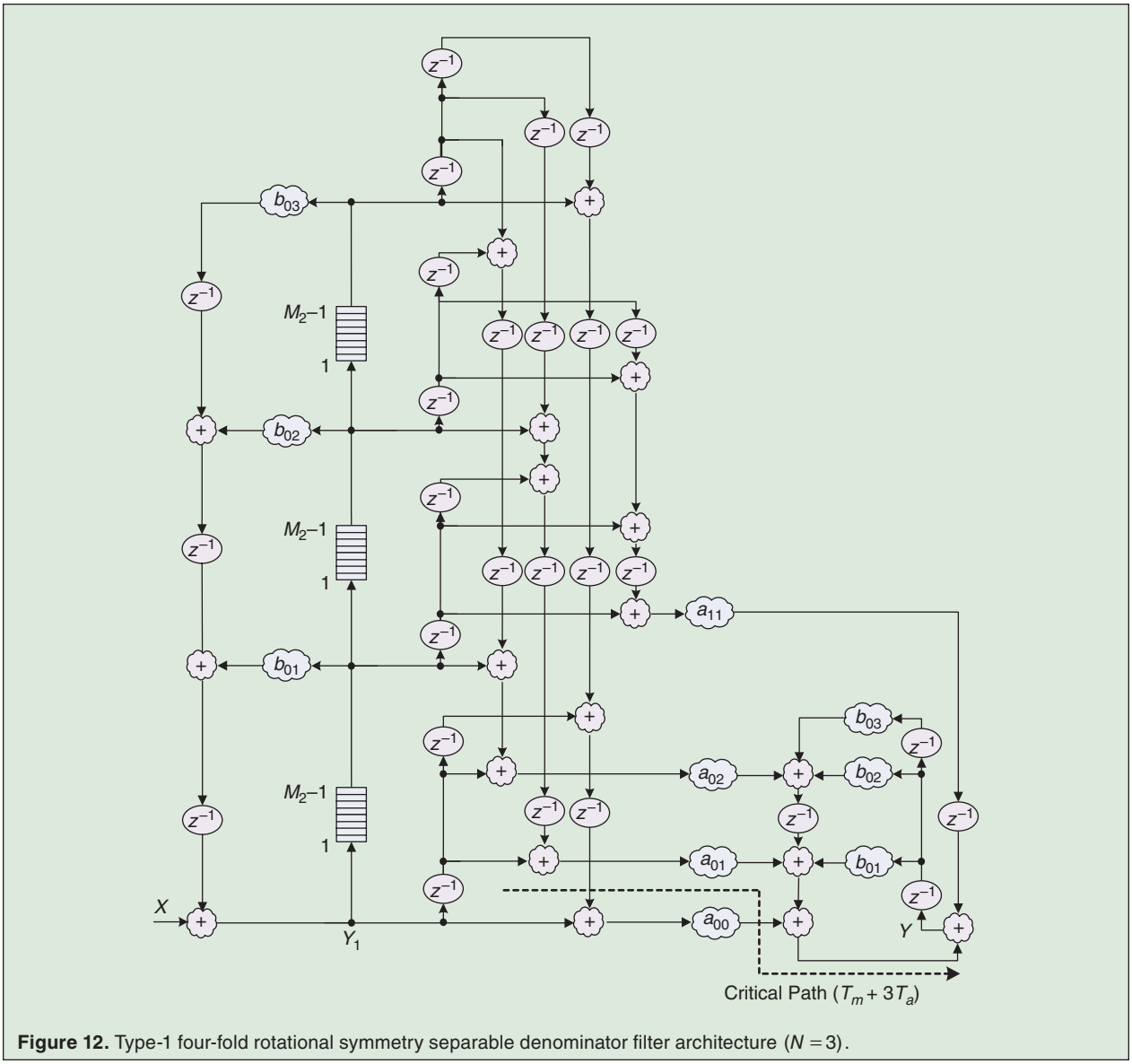


Figure 12. Type-1 four-fold rotational symmetry separable denominator filter architecture ($N = 3$).

for all i, j, k. So, for octagonal symmetry, with eqn. (19) unchanged, the output Y in (20) can be expressed as:

$$
\begin{aligned}
Y = & \sum_{j=1}^{N} b_{0j} z_2^{-j} Y + v a_{uu} z_1^{-u} z_2^{-u} Y_1 \\
& + v \cdot \sum_{i=0}^{u-v} a_{iu} (z_1^{-i} z_2^{-u} + z_1^{-u} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-(N-u)} + z_1^{-(N-u)} z_2^{-i}) Y_1 \\
& + \sum_{i=0}^{u-v} a_{ii} (z_1^{-i} z_2^{-i} + z_1^{-i} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-i}) Y_1 \\
& + \sum_{i=0}^{u-v-1} \sum_{j=i+1}^{u-v} a_{ij} (z_1^{-i} z_2^{-j} + z_1^{-i} z_2^{-(N-j)} + z_1^{-(N-i)} z_2^{-j} + z_1^{-(N-i)} z_2^{-(N-j)} \\
& \qquad + z_1^{-j} z_2^{-i} + z_1^{-j} z_2^{-(N-i)} + z_1^{-(N-j)} z_2^{-i} + z_1^{-(N-j)} z_2^{-(N-i)}) Y_1
\end{aligned}
\tag{27}
$$

Implementing the above, one can get the Type-1 octagonal symmetry filter architecture shown in Fig. 15. The Type-3 octagonal symmetry filter architecture is not shown here and can be found in [26]. The critical path analysis yields the delays of $T_m + 3T_a$ and $T_m + 2T_a$ respectively.

Due to symmetry, all six cost-effective filter architectures require fewer multipliers. The savings come from realizing the numerator of (16). The direct form implementation of the numerator with no symmetry (for $N = 3$) requires 16 multipliers. In the case of diagonal, quadrantal, four-fold rotational, octagonal symmetries, the number of multipliers needed are 10, 8, 4 and 3, respectively.

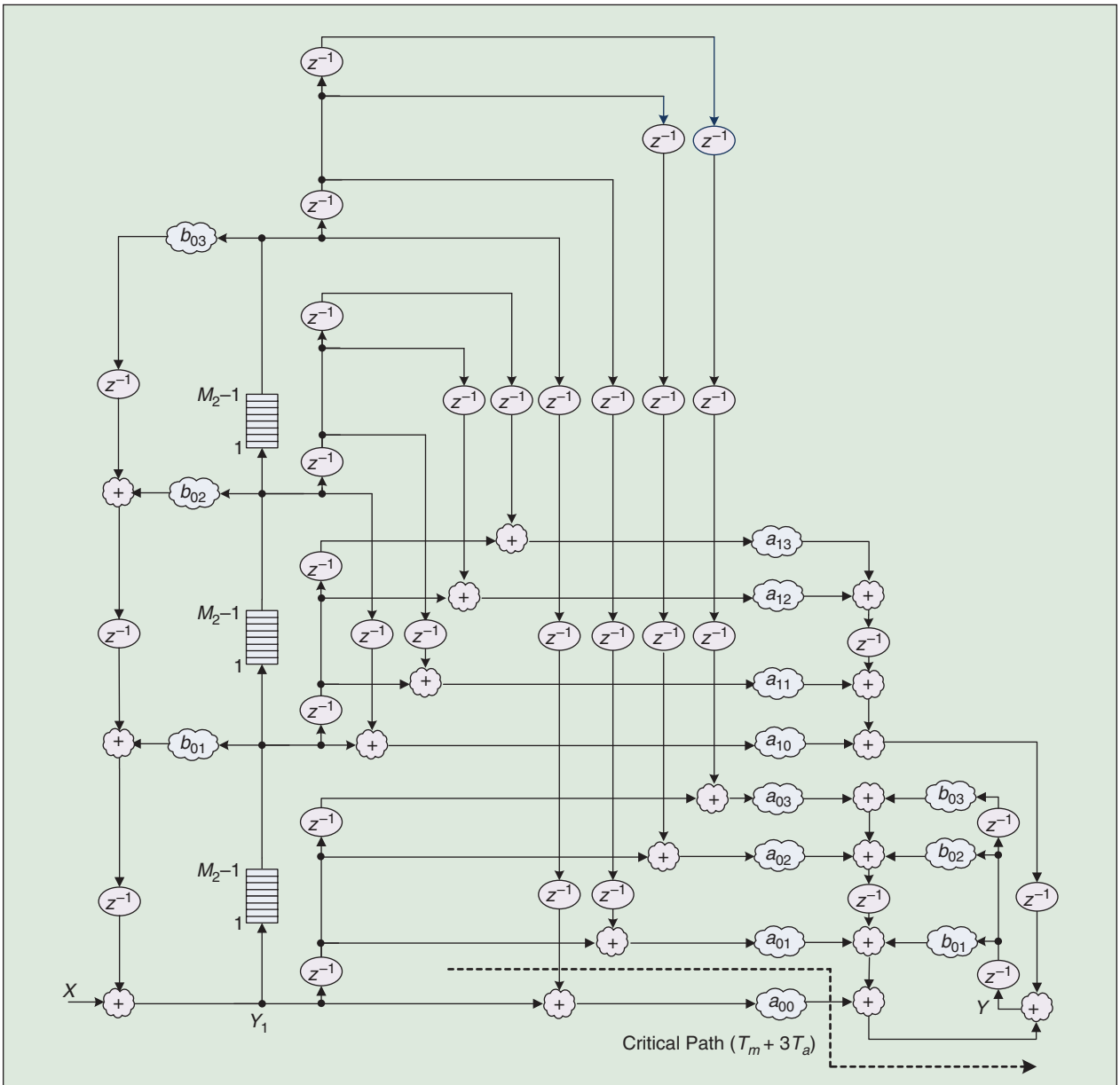


Figure 13. Type-1 quadrantal symmetry separable denominator filter architecture ($N = 3$).

The 2-D octagonal symmetry structure in Fig. 15 has the lowest number of multipliers.

V. Cost-Effective Multimode 2-D Filter Architecture Incorporating Four Symmetries

To reduce the cost of filter area and to increase hardware flexibility, two multimode filter architectures are developed that each supports four different symmetry modes: diagonal symmetry mode (DSM), four-fold rotational symmetry mode (FRSM), quadrantal symmetry mode (QSM), and octagonal symmetry mode (OSM). These two cost-effective multimode 2-D IIR filter architectures are shown in Fig. 16 and Fig. 17 for $N = 3$.

The cost-effective multimode 2-D symmetry filter architecture in Fig. 16 [20] can be derived based on three observations. First, the signal paths are added before the a_{ij} independent coefficient multiplier for the Type-1 symmetry filters in Figs. 10, 12, 13, and 15. Second, it can be

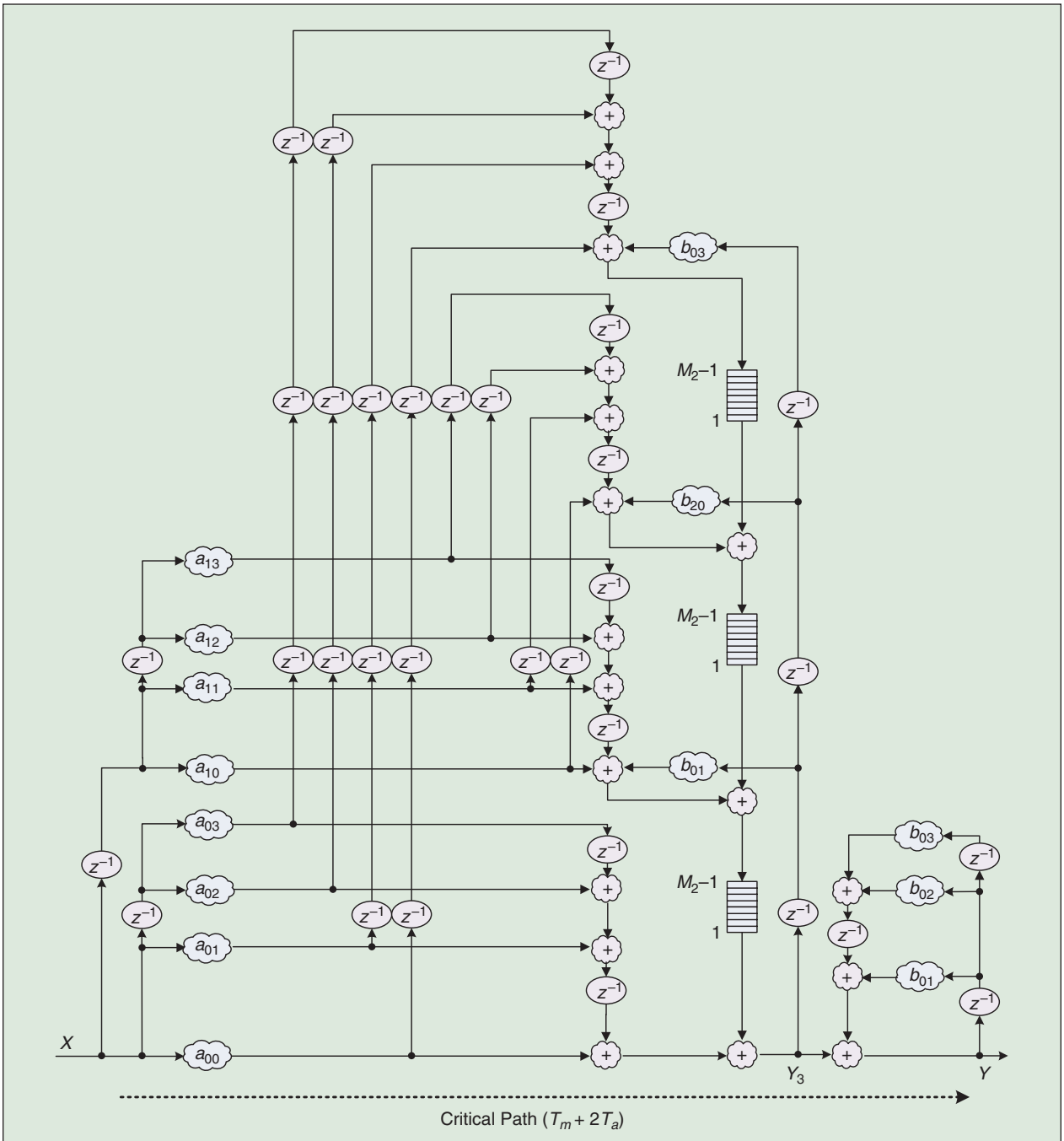


Figure 14. Type-3 quadrantal symmetry separable denominator filter architecture ($N = 3$).

seen from (18) that the Type-1 symmetry filter consists of two transfer functions: Y_1/X and Y/Y_1, with the Y_1/X transfer function being the same for the four individual symmetry filters as shown in (19). The block diagram of Y_1/X is depicted as Block 1 on the left-hand side of Fig. 16(a). Block 1 requires 3 multipliers and 3 adders. Next, we consider the Y/Y_1 transfer function which is different for each of the four individual symmetry filters. To construct Block 2 of the multimode filter, we need 3 multipliers for the denominator $\{b_{01}, b_{02}, b_{03}\}$, and 11 multipliers for the numerator $\{a_{00}, a_{01}, a_{02}, a_{03}, a_{10}, a_{11}, a_{12}, a_{13}, a_{22}, a_{23}, a_{33}\}$. Therefore, $11+3=14$ coefficient multipliers are required in Block 2 of Fig. 16(a) to achieve the operations for four different transfer functions of Y/Y_1. In terms of the number of adders from the architecture viewpoint, for Y/Y_1 of the multimode 2-D symmetry filter, 13 adders and 11 adders are needed on the left-hand side and right-hand side of Block 2 in Fig. 16(a), respectively.

In summary, the Type-1 multimode 2-D symmetry filter requires altogether 17 coefficient multipliers and 27 adders. Also, in Figs. 10, 12, 13, and 15, the interconnection control is only needed for the four Y/Y_1 transfer functions. The multiplication connections and internal connections are controlled by interconnection boxes (IBs) to accomplish the four-mode operations, where IB performs either connection or disconnection task for each signal path. According to the connections of the four individual symmetry filter architectures, 12 IBs are needed for the internal connections in Block 2. Therefore, based on the three observations mentioned above, the Type-1 multimode 2-D IIR filter with four symmetry modes can be obtained in Fig. 16(a). The interconnections difference among the four configurations of the

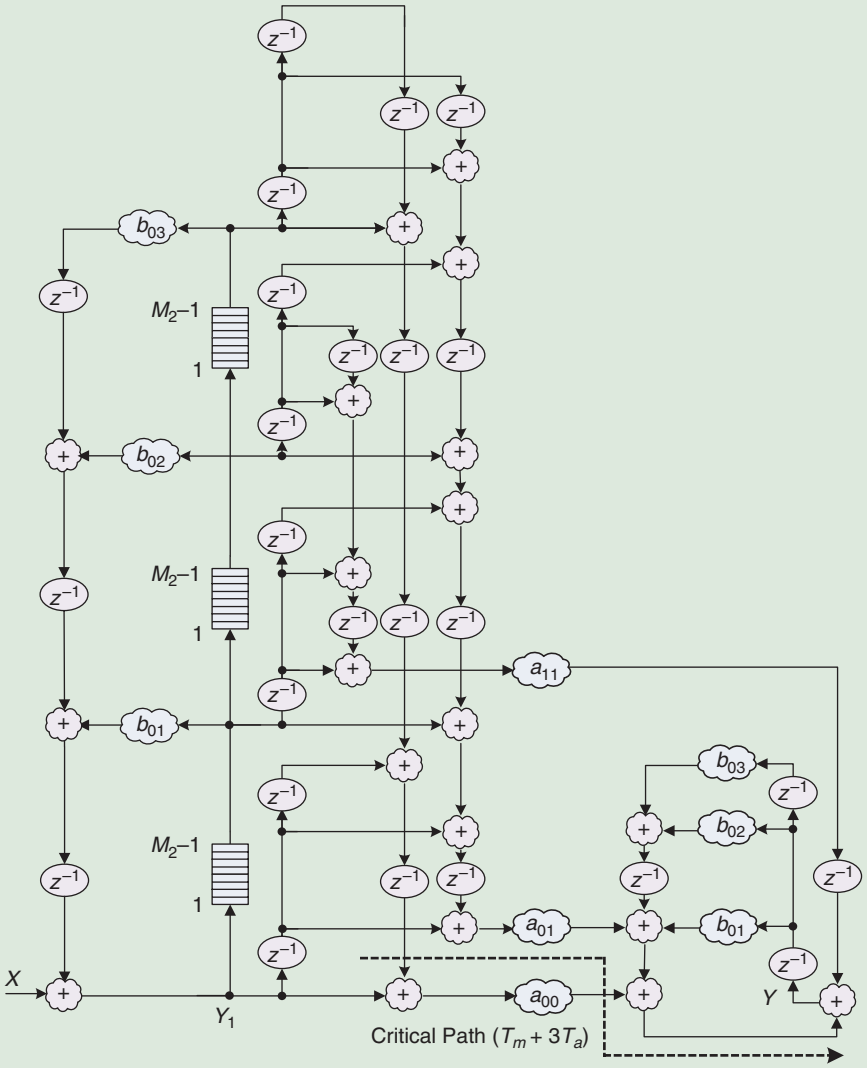
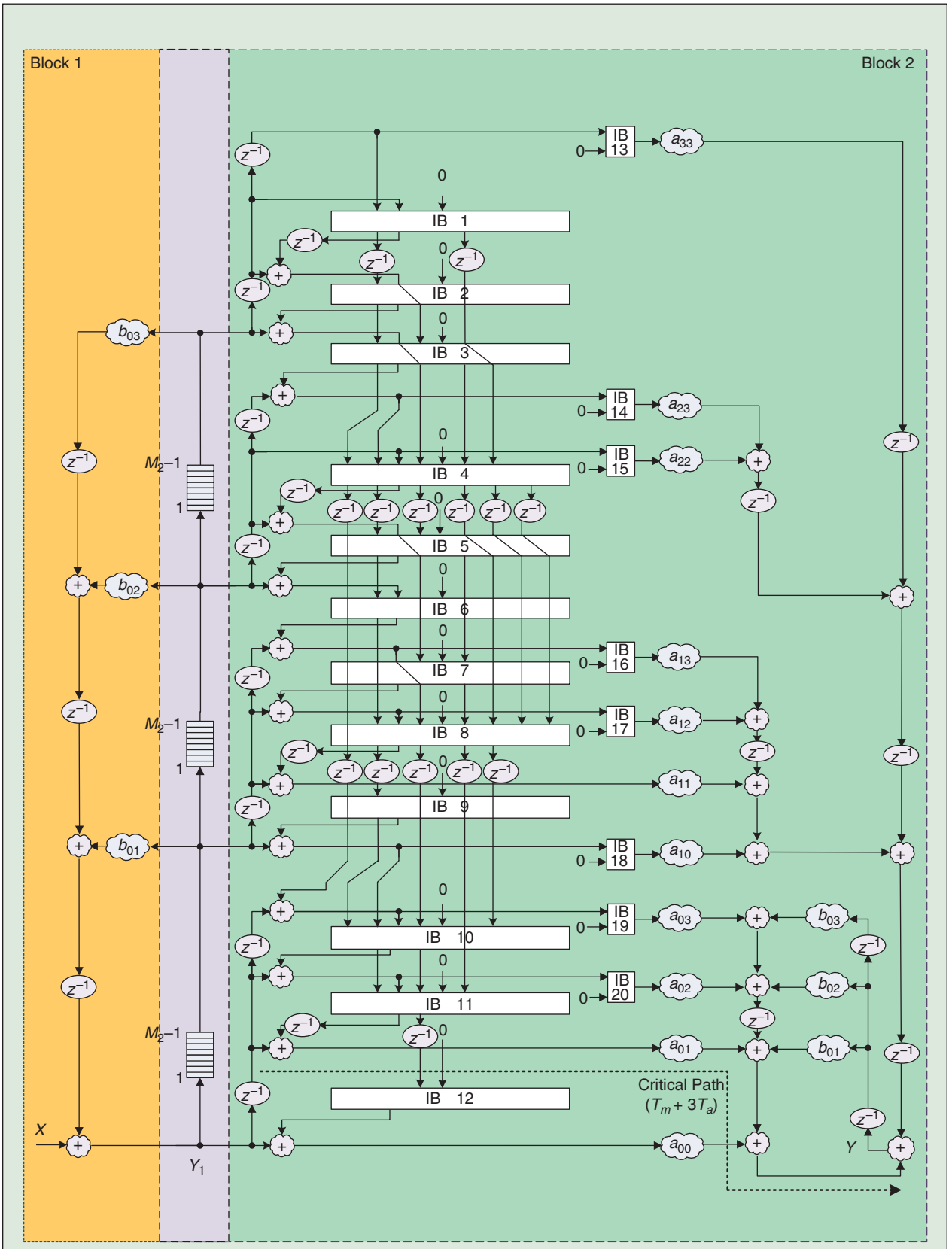


Figure 15. Type-1 octagonal symmetry filter architecture ($N=3$).



(a)

Figure 16. (a) Type-1 multimode 2-D IIR filter architecture with four symmetries for ($N = 3$); *(Continued)*

multimode filter architecture is highlighted in Fig. 16(b). The multimode filter architecture has a critical path of $T_m + 3T_a$ as shown in Fig. 16(a) by using the tree method.

Similarly, to support multiple symmetry functions, the Type-3 multimode 2-D IIR filter architecture giving (DSM, FRSM, QSM and OSM) modes of operation has been obtained and is given in Fig. 17 [25]. The details of this multimode structure can be found in [25]. Type 3 multimode filter architecture shown in Fig. 17(a) has a critical path of $T_m + 2T_a$.

The multimode architecture presented can support four different symmetry modes with just a slight area overhead. It achieves a multiplier reduction of 65.3% for $N = 3$ compared with the sum of the multipliers of the four individual symmetry filter structures thus making the multimode hardware architectures quite cost effective.

VI. Error Analysis for 2-D Symmetry Filter Architectures

The product quantization errors propagating through the filter architecture in fixed-point implementation have been studied in [3], [27]. Using the same approach here, the round-off noise errors for the Type-1 and Type-3 filter architectures are analyzed in [25] [26]. In the analysis, the round-off noise sources are assumed to be uncorrelated, wide-sense stationary and uniformly distributed, which allows linear decomposition to be applied. Furthermore, the noise source and the noise source with delay are regarded as independent.

For the Type-1 diagonal symmetry filter architecture in Fig. 10, the linear error signals e_1 and e_2 are given by:

$$e_1 = \sum_{j=1}^{N} e_{b0j} \tag{28}$$

$$e_2 = \sum_{j=1}^{N} e_{b0j} + \sum_{i=0}^{N} e_{aii} + \sum_{i=0}^{N-1} \sum_{j=i+1}^{N} e_{aij} \tag{29}$$

Since e_1 error/noise source passes through the whole filter architecture and e_2 passes through b_{0j} at the right-hand side in Fig. 10, total variance of quantization error of the Type-1 diagonal symmetry filter architecture can be derived as:

$$\sigma^2_{\text{Type1\_Dia}} = N\sigma_e^2 \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} |h[m,n]|^2 + \left(2N + 1 + \frac{N(N+1)}{2}\right)\sigma_e^2 \sum_{n=-\infty}^{\infty} |h_{b2}[n]|^2 \tag{30}$$

where $\sigma_e^2 = 2^{-2B}/12$, B is the fractional bit width after quantization, and and $h_{b12}[m,n]$ are defined as:

$$h_{b2}[n] \xleftrightarrow{z} \frac{1}{1 - \sum_{j=1}^{N} b_{0j} z_2^{-j}} \tag{31}$$

$$h_{b12}[m,n] \xleftrightarrow{z} \frac{1}{\left(1 - \sum_{i=1}^{N} b_{0i} z_1^{-i}\right) \cdot \left(1 - \sum_{j=1}^{N} b_{0j} z_2^{-j}\right)} \tag{32}$$

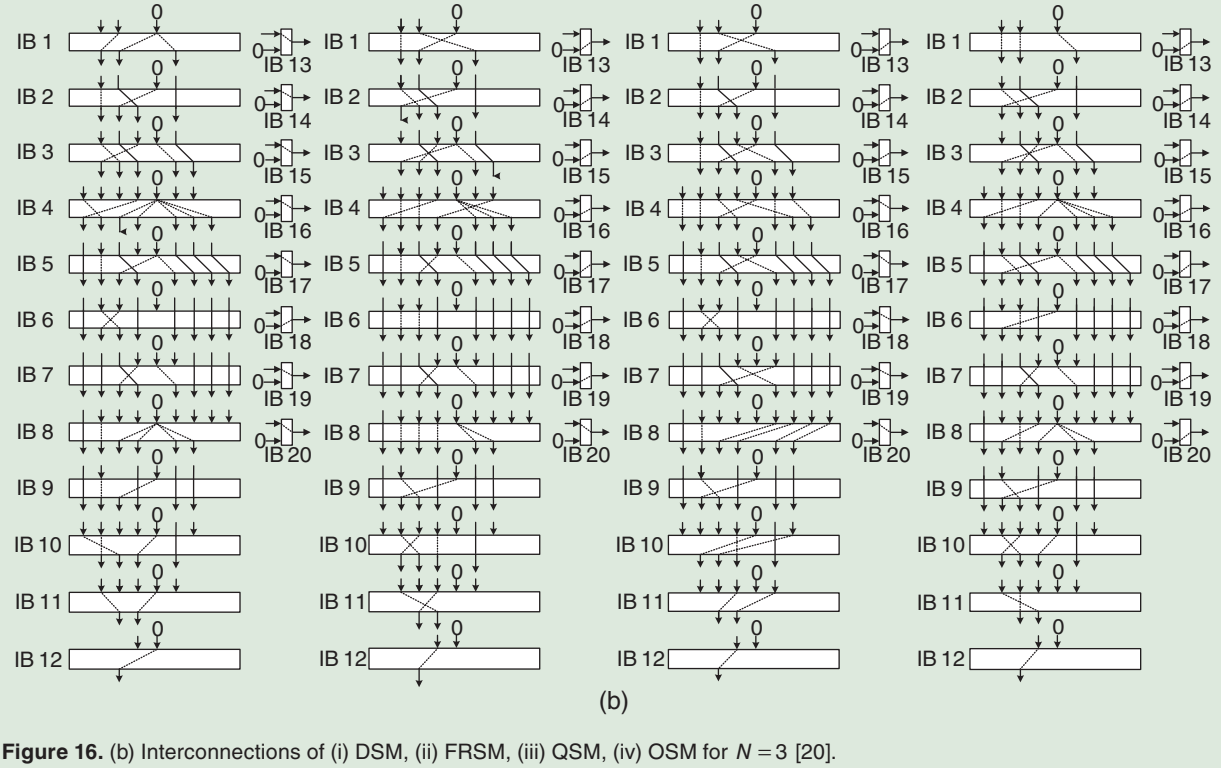
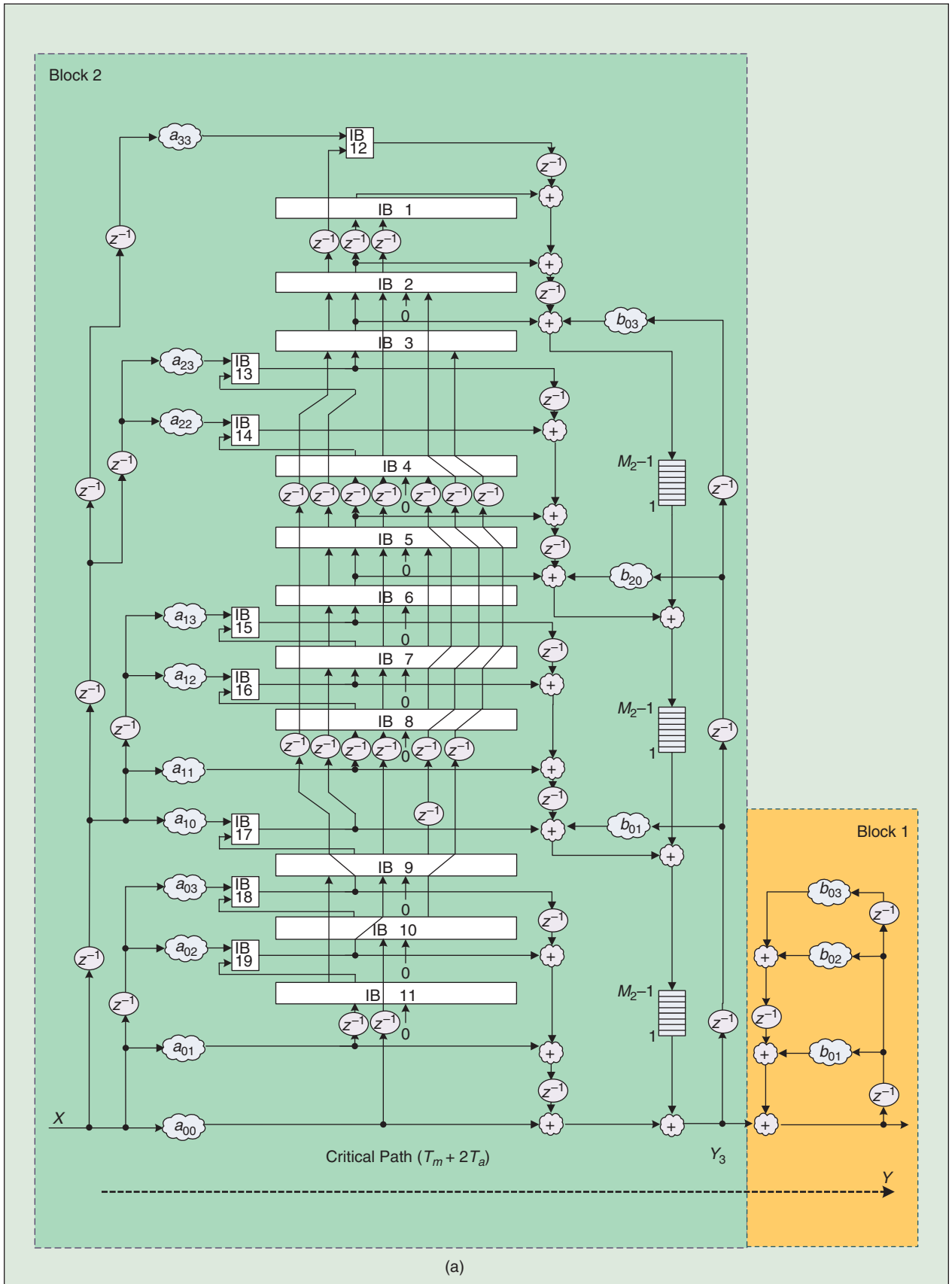


Figure 16. (b) Interconnections of (i) DSM, (ii) FRSM, (iii) QSM, (iv) OSM for $N = 3$ [20].



(a)

Figure 17. (a) Type-3 multimode 2-D IIR filter architecture with four symmetries for ($N = 3$); *(Continued)*

For comparison, the error analyses of Type-1 four-fold, quadrantal symmetry and octagonal symmetry filter architectures are listed below.

$$\sigma^2_{\text{Type1\_FF}} = N\sigma_e^2 \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} |h[m,n]|^2 + (N+v+(u-v+1)(N-u+v))\sigma_e^2 \times \sum_{n=-\infty}^{\infty} |h_{b2}[n]|^2 \quad (33)$$

$$\sigma^2_{\text{Type1\_Qua}} = N\sigma_e^2 \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} |h[m,n]|^2 + [N+v(N+1)+(u-v+1)(N+1))]\sigma_e^2 \times \sum_{n=-\infty}^{\infty} |h_{b2}[n]|^2 \quad (34)$$

$$\sigma^2_{\text{Type1\_Oct}} = N\sigma_e^2 \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} |h[m,n]|^2 + [N+v+v(u-v+1)+(u-v+1) + (u-v)(u-v+1)/2]\sigma_e^2 \sum_{n=-\infty}^{\infty} |h_{b2}[n]|^2 \quad (35)$$

Similarly, the total variance of quantization error of Type-3 symmetry filter architectures is derived as

$$\sigma^2_{\text{Type3\_Dia}} = \sigma^2_{\text{Type3\_FF}} = \sigma^2_{\text{Type3\_Qua}} = \sigma^2_{\text{Type3\_Oct}} = N\sigma_e^2 \sum_{n=-\infty}^{\infty} |h_{b2}[n]|^2 + [N+(N+1)^2]\sigma_e^2 \times \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} |h_{b12}[m,n]|^2 \quad (36)$$

where $h_{b2}[n]$ and $h_{b12}[m,n]$ are defined in (31) and (32) respectively.

VII. Implementation and Comparison of Results

As proof of concept, the chip layout of Type-1 multimode 2-D IIR filter architecture in Fig. 16 is shown in Fig. 18. The circuit has a size of 718.95 μm $\times$ 711.05 μm and an average power consumption of 29.34 mW. As indicated in [20], compared with the sum of the areas of the four individual symmetry filters, the area saving could be up to 63.25%. The details of the architecture comparison in terms of the number of multipliers, number of adders, and critical path are shown in Table 1.

The Type-3 symmetry filter architectures also possess shorter critical path delay than the Type-1 symmetry filter architecture. In terms of adders, it is known that the area of an adder is much less than that of a multiplier. To achieve fair comparison, the n-bit adder can be equivalently evaluated as $1/n$ $n \times n$-bit multiplier using array multiplier approach [28]. According to the hardware implementation in [20], 16×16-bit multiplier and 16-bit full-adder with two inputs are reasonable assumptions to realize this design. The Type-3 multimode 2-D filter architecture not only has less critical path delay but also has lower number of adders than the Type-1 multimode 2-D filter architecture.

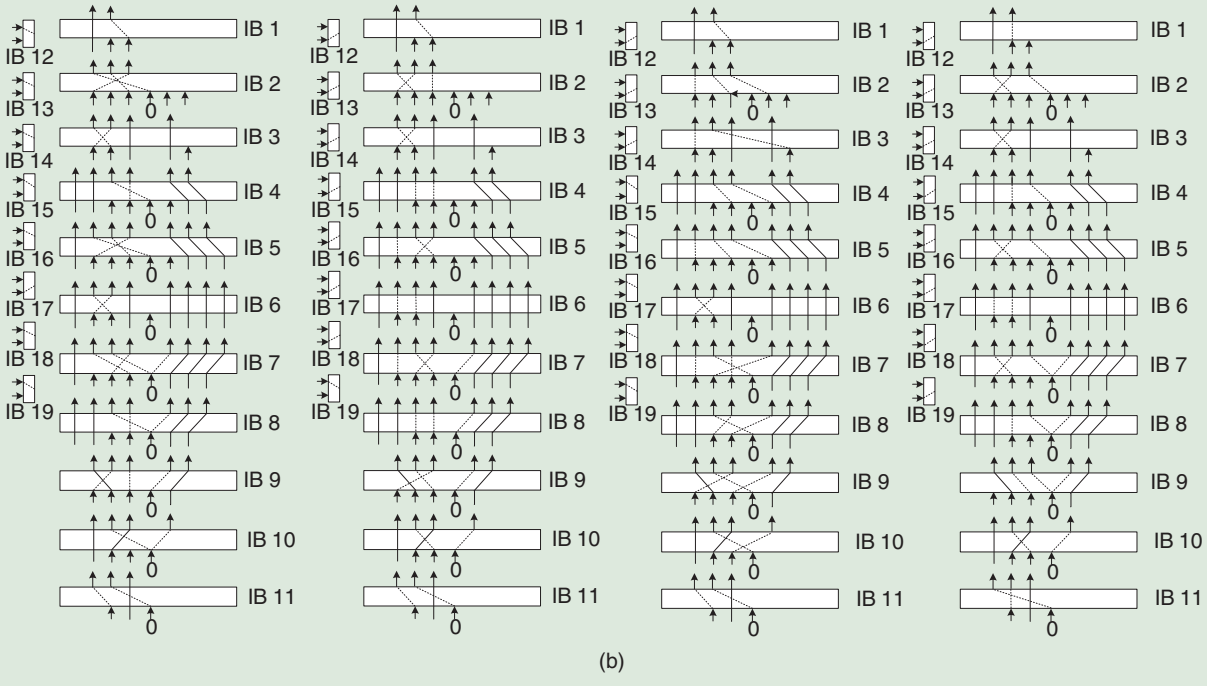


Figure 17. (b) Interconnections of (i) DSM, (ii) FRSM, (iii) QSM, (iv) OSM for $N = 3$ [25].

VIII. Filter Design Example

Consider a design example for a narrowband Fan filter with diagonal symmetry. The filter magnitude specification is shown in Fig. 19. The filter passband has an angle $\phi_1 = 15$ deg and the transition band has an angle $\phi_2 = 10$ deg. (Note that the specs only show $\theta_2 > 0$ for the vertical axis). A 2-D Fan filter can be used in the design of 3-D cone filters which see applications in high-selectivity beam formers [15].

Optimization is used to obtain the transfer function that satisfies the Fan filter specification. The form of the transfer function (with unknown coefficients) chosen satisfies the diagonal symmetry as the given Fan filter specs exhibit diagonal symmetry. The objective is to minimize sum of the squared errors between the filter magnitude response and the given filter specifications evaluated on a uniform raster in the 2-D frequency plane. The objective or error function is shown in (37). It is based on the difference between the magnitude response of the transfer function and the desired magnitude response, at selected frequency points in both the passband and stopband.

$$\text{Error} = \sum_k \sum_l [F(\theta_{1k}, \theta_{2l}) - F_d(\theta_{1k}, \theta_{2l})]^2 \qquad (37)$$

where F is the transfer function magnitude squared response, F_d is the desired response, and θ_{1k}, θ_{2l} are the sample frequency points where the desired response is specified.

The design is done using a (variable) separable denominator transfer function as described in Section III. The optimization results, for different filter orders, are shown in Table 2. The 3-D surface plot for order 5×5 is shown in Fig. 20. The contour plots for orders (5×5) and (3×3) are given in Fig. 21. As expected, with higher filter order,

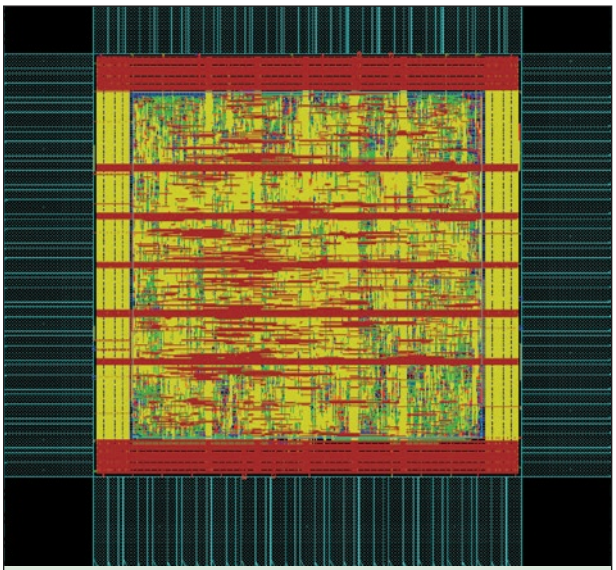


Figure 18. Chip layout of the Type-1 multimode 2-D symmetry filter for $N = 3$ [20].

Table 1.
Comparison of different 2-D IIR filter architectures with the order N.

Works		# of Multipliers	# of Multipliers for $N=3$ #	# of Multipliers for $N=3$ %	# of Adds with two inputs for $N=3$ #	# of Adds with two inputs for $N=3$ Equivalent # of 16×16-bit mul.	Critical Path
Van [13]		$2(N+1)^2-1$	31 for Gen	100%	30	1.875	T_m+3T_a
Separable Denominator	Type-1	$(N+1)^2+2N$	22	70.97%	21	1.3125	T_m+3T_a
	Type-3						T_m+2T_a
Diagonal	Type-1	$\frac{1}{2}(N+1)^2+\frac{5}{2}N+\frac{1}{2}$	16	51.61%	21	1.3125	T_m+3T_a
	Type-3						T_m+2T_a
Four-Fold Rotational	Type-1	$\frac{1}{4}(N+1)^2+\frac{3}{4}v+2N$	10	32.26%	21	1.3125	T_m+3T_a
	Type-3						T_m+2T_a
Quadrantal	Type-1	$\frac{1}{2}(N+1)^2+\frac{v}{2}(N+1)+2N$	14	45.16%	21	1.3125	T_m+3T_a
	Type-3						T_m+2T_a
Octagonal	Type-1	$\frac{1}{8}(N+1+v)^2+\frac{1}{4}(N+1+v)+2N$	9	29.03%	21	1.3125	T_m+3T_a
	Type-3						T_m+2T_a
Type-1 Multimode		$\frac{1}{2}(N+1)^2+\frac{1}{2}(N+1)+\frac{1}{8}(N+1+v)^2$	17	54.84%	29	1.8125	T_m+3T_a
Type-3 Multimode		$-\frac{1}{4}(N+1+v)+2N$			21	1.3125	T_m+2T_a

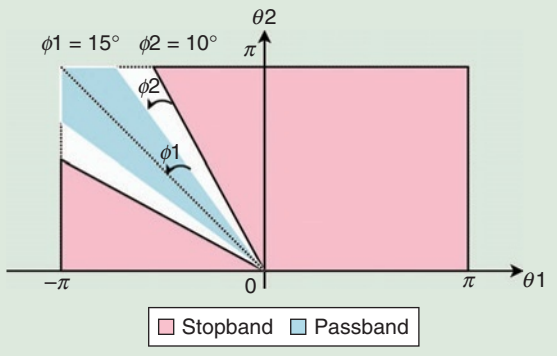


Figure 19. Fan filter specification.

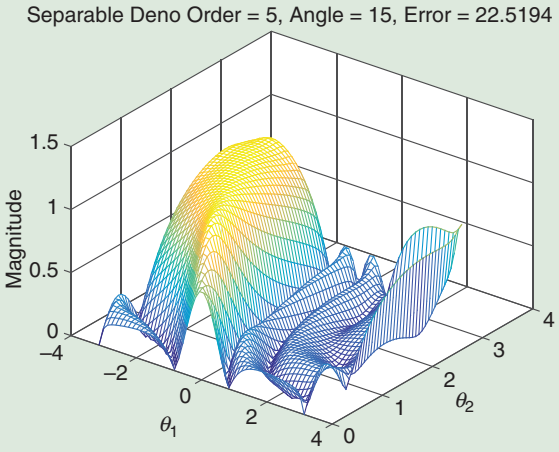


Figure 20. 3-D surface plot for separable denominator Fan filter with order 5 x 5.

Table 2.
Separable denominator design.

Filter order	Design error	# of multipliers
5×5	22.5	31
4×4	29.1	23
3×3	44.6	16

the design error is reduced. But the tradeoff is the greater number of multipliers required in the final filter structure.

As previously mentioned, for the diagonal symmetry, the denominator of the 2-D filter transfer function need not be separable. For the sake of the completeness of the structures, order 2×2 non-separable denominator filter structure possessing diagonal symmetry is shown in Fig. 22. The critical path analysis yields the delay of $T_m + 2T_a$. The number of multipliers saved compared to non-symmetric implementation [13] by direct form is six. This order 2×2 structure can be extended for a filter of any order. In general, the number of multipliers required in a non-separable denominator filter structure with diagonal symmetry is $N^2 + 3N + 1$. Without any symmetry, the number of multipliers required is $2N^2 + 4N + 1$.

IX. SUMMARY

This review article written as a dedication to the memory of Professor Alfred Fettweis gives the most recent update of the research results connected with 2-D digital filter structures possessing symmetry. The symmetries incorporated in these VLSI implementable architectures are: quadrantal, diagonal, four-fold rotational and octagonal. Cost effective multimode symmetry architectures combining the above symmetry modes of operation are presented. The error analysis of the structures and the

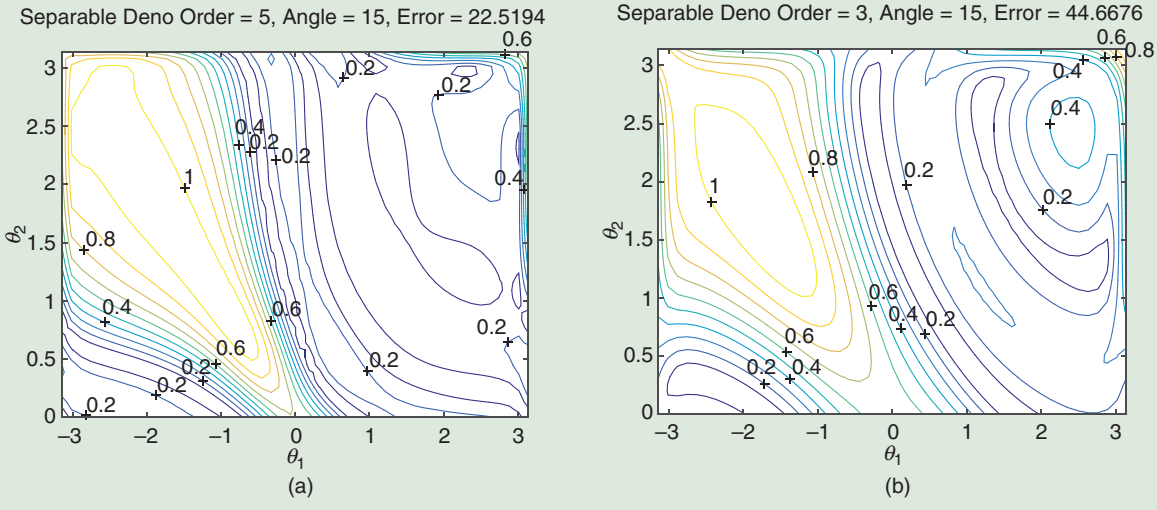


Figure 21. Contour plots for separable denominator Fan filter with order (a) 5×5 and (b) 3×3.

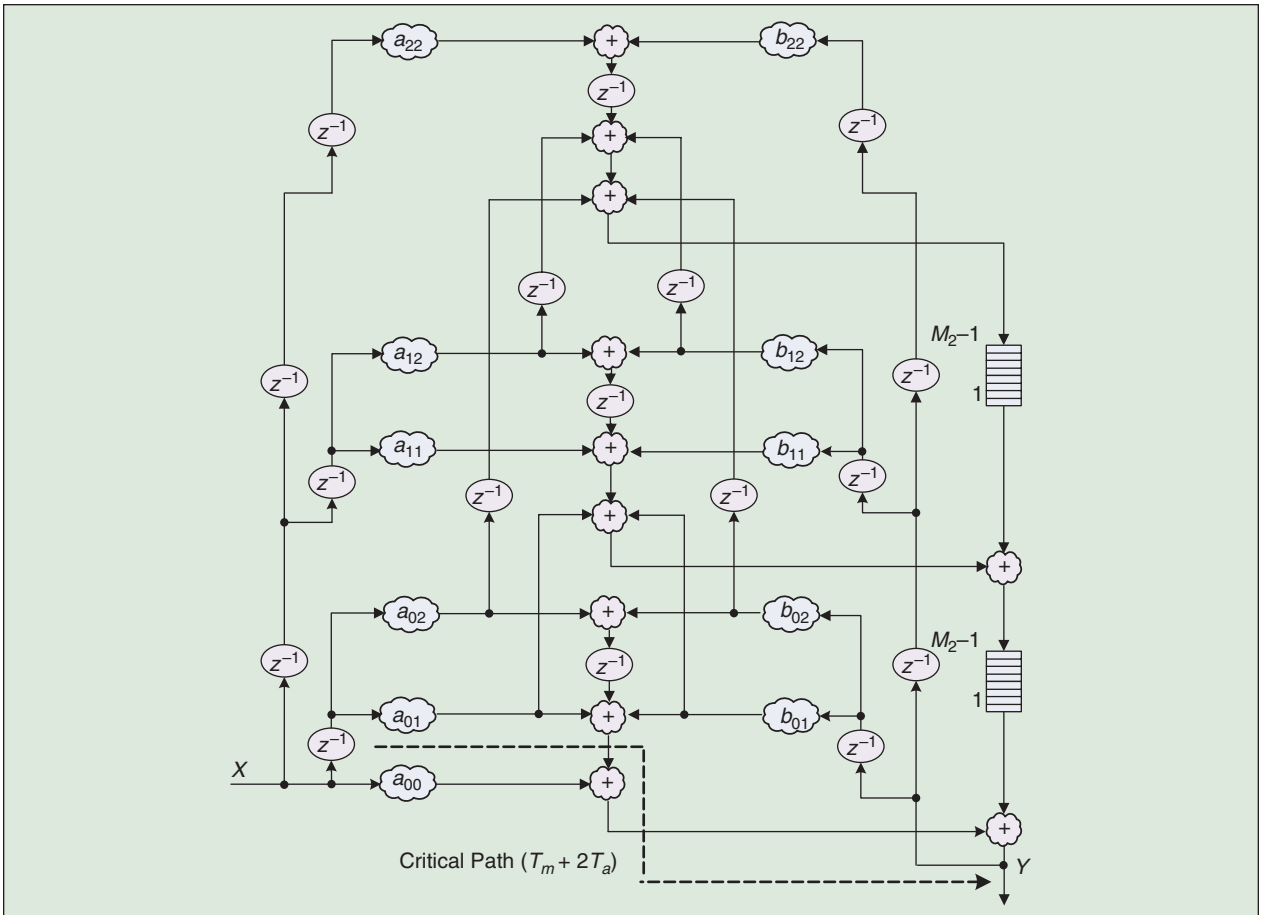


Figure 22. Degree 2×2 non-separable denominator filter structure with diagonal symmetry.

implementation aspects are also discussed. A Fan filter design with diagonal symmetry is presented in the end along with a filter structure for a 2-D transfer function with diagonal symmetry. By utilizing the generalized design procedure and using sub-networks and frameworks, the individual symmetry and multimode filter architecture for any order could be obtained.

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Lan-Da Van (S'98-M'02-SM16) received the Ph. D. degree from National Taiwan University (NTU), Taipei, Taiwan, in 2001 in electrical engineering. From 2001 to 2006, he was with the National Chip Implementation Center (CIC), Hsinchu, Taiwan. In 2006, he joined the faculty of the Department of Computer Science, National Chiao Tung University (NCTU), Taiwan, and is currently an Associate Professor. He is now the Deputy Director of NCTU M2M/IoT R&D Center. His research interests are in digital signal processing and learning computation algorithms, architectures, chips, systems and applications. He received the Best Paper Award in the IEEE iThings2014. He has also received the teaching award of Computer Science College, NCTU in 2014. Dr. Van served as Chairman of the IEEE NTU Student Branch in 2000 for which he has received the IEEE Award for outstanding leadership and service. From 2009 to 2010, he served as an Officer of the IEEE Taipei Section. In 2014, he was a Track Co-Chair of the 22nd IFIP/IEEE VLSI-SoC. He also was a Track Co-Chair of the 2018 IEEE MWSCAS and a Special Session Co-Chair of the 2018 IEEE International Conference on DSP. Professor Van is an Associate Editor for the IEEE Transactions on Computers (2014~2018) and an Associate Editor for the IEEE Access (2018~present).

I-Hung Khoo (M'03) received his Ph.D. in Electrical and Computer Engineering from the University of California Irvine in 2002. He is currently a professor in the Department of Electrical Engineering and the Department of Biomedical

Engineering at California State University Long Beach. Previously, he was a Senior I. C. Design Engineer at Agilent/Avago Technologies. Dr. Khoo's research interests include high speed circuit design, analog & digital signal processing, and biomedical circuits and devices.

Pei-Yu Chen (S'10) was born in Taipei, Taiwan. She received the B.S. and M.S. degrees in engineering and system science from National Tsing Hua University (NTHU), Hsinchu, Taiwan, in 2004 and 2007, respectively. She received Ph.D. degree from National Chaio Tung University (NCTU), Hsinchu, Taiwan, in 2018. Her research interests include multidimentional signal processing and VLSI design.

Haranatha (Hari) C. Reddy (M'77-SM'82-F'92-LF2010) received his Ph.D. in Electronics and Communications Engineering from Osmania University, Hyderabad, India in 1974 and then did two years of Post-Doctoral research at Concordia University, Montreal, Canada. He is now a Professor (emeritus) at the California State University, Long Beach, California and an adjunct professor at the University of Victoria, Canada. He has been a visiting chair professor at NCTU, Taiwan since 2007. Earlier, he held visiting appointments at ETH Zurich, Switzerland; Concordia University, Montreal, Canada and at the University of California, Irvine, CA. His research interests and publications for the past 40 years has been in multidimensional circuits, filters and signal processing area. He is now a Life Fellow of the IEEE. Professor Reddy has over the years served the IEEE Circuits and Systems society in many capacities including serving as the President of the CAS Society in 2001. He is the recipient of the 2003 Meritorious Service award from the IEEE CAS Society.

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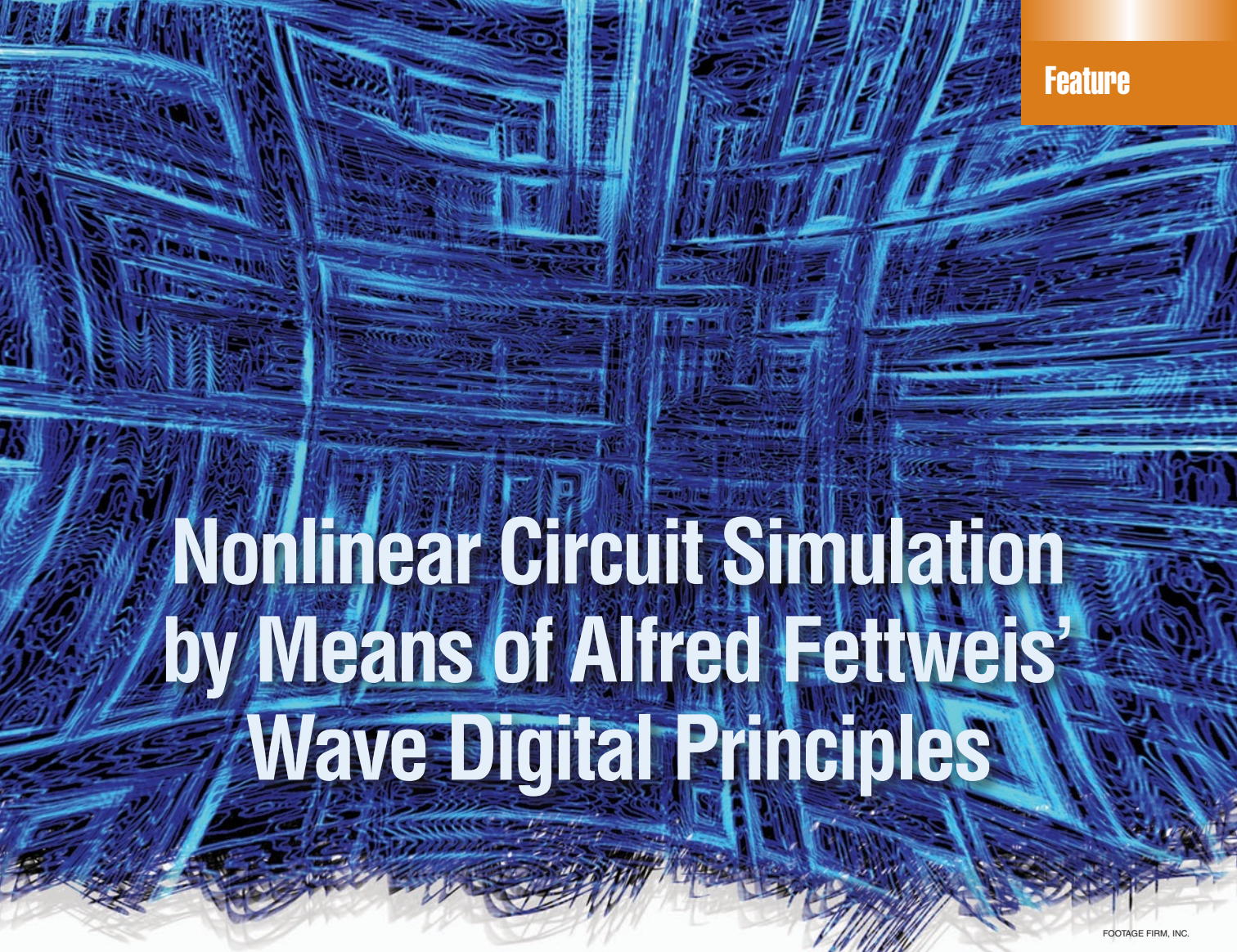

Nonlinear Circuit Simulation by Means of Alfred Fettweis' Wave Digital Principles

FOOTAGE FIRM, INC.

Tim Schwerdtfeger and Anton Kummert

Abstract

A dependable circuit simulation plays an elementary part in the process of commercial circuit design. However, when Alfred Fettweis invented the concept of Wave Digital Filters (WDFs) back in the early 1970s, that was clearly not the case as tools like SPICE hadn't been published yet. But even though Fettweis' new WDFs were able to provide an accurate digital model of analogue reference circuits, they were mostly perceived as an elaborated technique for digital filter design. In this article we provide an insight into Wave Digital Filters with a focus on nonlinear circuit simulation, highlighting assets and drawbacks of the method. In particular, recent results that extend the Wave Digital concept towards a general circuit simulation strategy with interesting properties are presented.

I. Introduction

In the early days of Digital Signal Processing, Alfred Fettweis introduced the concept of Wave Digital Filters (WDFs) to obtain a class of recursive digital filters that is directly related to analogue reference circuits [1]–[2]. The basic approach is both elegant and powerful, as it directly utilizes general results from network theory. As we'll see in the following, WDFs are a direct application of scattering matrix theory that mostly goes back to Vitold Belevitch [3], who also happened to be a steady supporter for Alfred Fettweis' scientific career. To give a starting point into the topic, first the Wave Digital Concept is presented briefly. For an in-depth tutorial, please refer to Fettweis' publication [2] or, more conveniently, to Klaus Meerkötter's article in this very issue.

A. The Wave Digital Concept

Wave Digital structures exhibit some remarkable properties like high numerical robustness, real-time capability by definition, and, as passive building blocks are used exclusively, general stability [4]. The concept has a wide application spectrum ranging from classic signal processing tasks, e.g. audio applications, to numerical solving of partial differential equations [5]–[7]. The

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At first glance, Fettweis' Wave Digital Concept seems to be the perfect solution to circuit simulation: it's strictly modular, it's robust and it's fast.

construction principles are strictly modular: all electrical elements of a given prototype Kirchhoff circuit are discretized individually into their Wave Digital counterparts which, subsequently, are combined into the final digital structure. For this purpose, a given analogue reference network has to be decomposed into one-port elements like resistors, capacitors, inductors and voltage sources on the one hand, and, on the other hand, the underlying network topology in form of parallel and serial interconnections of the elements. The basic idea to obtain a realisable signal-flow graph from the determinant Kirchhoff quantities of current i and voltage u which are measurable through and across each element, is to transform the latter into directional wave variables

$$\begin{aligned} a &= u + Ri \\ b &= u - Ri, \end{aligned} \tag{1}$$

with incident and reflected waves a and b, respectively, as well as a port resistance parameter $R > 0$. The above definition of wave variables has the unit of voltages and is the most common, but equivalent representations as current or power waves are available, as well. This kind of bidirectional description of an electrical one-port is quite common in high-frequency engineering but is valid down to DC applications.

In conjunction with the discretization by means of the bilinear transformation (better known as the discrete trapezoidal rule), a lot of basic electrical elements can now be translated into their Wave Digital counterparts: A capacitor corresponds to a simple unit delay element, for example, whereas a resistor is realized as a signal sink which now implements the dissipation of the analogue element in the Wave Digital domain. For a more extensive list please refer to [2].

In a similar fashion to the derivation of the atomic Wave Digital elements, modular building blocks are defined to realize their connection: so-called adaptor blocks are derived from the application of the wave variable definition to the Kirchhoff laws that describe the network topology. Usually, while other definitions are possible, adaptors represent three-port parallel and serial connections. In classic network theory, such an adaptor corresponds to a lossless local scattering matrix that is parameterized by the connected electrical components. This matrix determines how much of an incident signal at a port is reflected directly or distributed (scattered) to the remaining ports.

As the last step, all Wave Digital elements and adaptors are combined into the final Wave Digital Filter. Local properties of the elements like their passivity are preserved and now extend to the global Wave Digital structure. This is remarkable on its own as with these principles recursive filter structures of arbitrary order can be derived that are always stable and are generally well-behaved in that they exhibit a high numerical robustness against different kinds of round-off errors [2]–[4]. More than that, the Wave Digital filter digitally emulates the analogue reference circuit with very high quality, as all internal states, its modularity and topology are preserved. Additionally, the computational complexity of Wave Digital Structures grows linearly with the number of elements simulated. In summary, there's a lot to like.

B. The Catch: Realization Without Delay-free Loops

At first glance, Fettweis' Wave Digital Concept seems to be the perfect solution to circuit simulation: it's strictly modular, it's robust and it's fast. On closer examination, however, there are some restrictions regarding the realizability of the synthesized Wave Digital Filters. Problem here: the connection of two elements in a WD structure is always *bidirectional* for which reason there may occur delay-free loops in the digital signal path that prevent an algorithmic realization. In fact, this corresponds to an *implicit* description of both reflected and transmitted signal portions at a port, which is perfectly fine from a mathematical point of view, but to obtain a realizable digital system, an *explicit* formulation is mandatory. Usually, this implicit relation is solved by stating that at least one of two connected WD ports is required to exhibit no direct reflection at all. For classic linear building blocks like capacitors, inductors, resistors or resistive sources, this can conveniently be realized by restricting the formerly free port resistance parameter R to the value of the actual element in Kirchhoff domain.

It gets more complicated, however, if we consider not just single electrical components, but also take their interconnection in form of adaptor blocks into account. The classic adaptors with three or more ports can be realized with a reflection-free port by forcing a diagonal entry of

T. Schwerdtfeger and A. Kummert are with the Faculty of Electrical, Information and Media Engineering at the University of Wuppertal, Germany.

the underlying scattering matrix to zero. In case of a serial adaptor, for example, this is achieved by choosing the port resistance of one port equal to the sum of the remaining ports, following the rules of straight forward impedance matching. Unfortunately, this procedure is applicable only once per adaptor. Thus, each multi-port adaptor may feature one reflection-free port *at most* which has a direct effect on the possible topologies of the resulting Wave Digital structure. In fact, this restriction of the number of reflection-free ports available dictates a *tree-like* structure to any classic Wave Digital Filter as depicted in figure 1. Here, reflection-free ports are marked with the usual symbol "⊥", all facing upwards to a common root node. The choice of three-port adaptors results in a binary connection tree [8], but the general tree structure holds for adaptors of arbitrary size. Within such a tree, the root element is of particular importance for the modelling of nonlinear reference circuits, as it is the only spot in the whole structure where a nonlinear element (or any element featuring a direct reflection, for that matter) can be accommodated. To be more precise, this not only excludes any reference circuits that contain multiple nonlinearities like diodes from the translation into a classic Wave Digital Filter, all multiport nonlinear elements like the important class of transistors are excluded entirely. To add insult to injury, the bad news don't stop here: the forced tree structure imposes serious restrictions on the realizable reference circuits, even in the linear case. For the most simple example, take the well-known bridged T-circuit in figure 2. The reformulation step to obtain something more manageable in terms of port-based parallel and serial connections yields the equivalent circuit depicted in figure 3: a ring-like topology which obviously does not fit into the connection tree scheme. The problem with this type of structure again are delay-free loops in a direct realization with adaptors, only this time they don't occur within a single port but on a macroscopic level which is just as effective in preventing an explicit algorithmic description.

To sum it up: the Wave Digital Concept is a unique approach that connects analogue circuits and digital systems in a completely modular fashion where each electrical element is discretized individually. In this procedure, a lot of the favourable properties of the reference circuit are maintained in the Wave Digital simulation, most notably its passivity, stability and great robustness. The weak spot of the classic approach lies within its lack of adaptability to important classes of reference circuits, thus a direct application of Wave Digital Filters as a *universal* circuit simulator is just not possible. Fortunately, recent advances in the community provide solutions to these restrictions to pave the way towards a universal circuit simulation based on Wave Digital Filters. These new extensions can be classified into two basic categories: approaches that combine the problematic part of the circuit into a secondary structure that has to be solved separately, and approaches that keep the modular character of the original Wave Digital Concept. We'll start with a brief

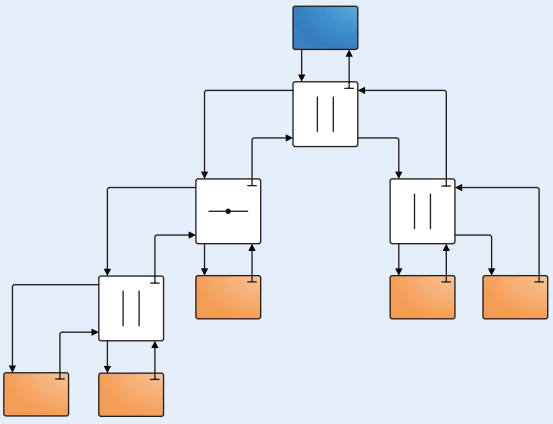

Figure 1. Typical tree structure of an example Wave Digital Filter to avoid the occurrence of delay-free loops.

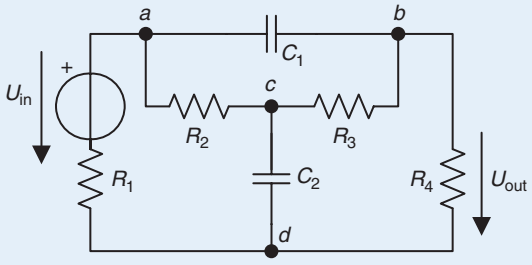

Figure 2. A simple Bridged T filter network.

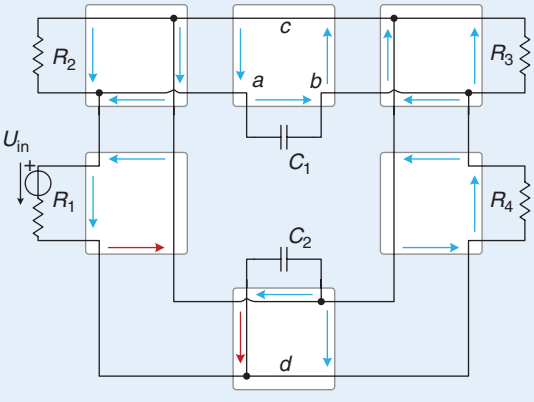

Figure 3. Bridged T circuit shown in figure 2 rearranged to emphasize the underlying parallel and serial connections. Note that node *c* is now represented by a loop which results in a ring-like structure. A direct implementation with WDF building blocks would contain delay-free loops. Coloured arrows indicate sign convention of the corresponding adaptor blocks, red denotes a mismatch between two adjacent blocks.

"So you've got a delay-free loop that you can't process, why not just put a delay into it?"

overview of selected non-modular techniques before discussing a strictly modular method in detail.

II. Non-Modular Approaches

If we exclude nonlinear elements for a moment, a straight forward method that sacrifices topology altogether but circumvents the WDF constraints is to use a direct implementation of the global scattering matrix of the circuit as part of a state space formulation. Except for idealized elements like a nullator, this matrix description exists for almost every circuit imaginable [3] and has been considered in the WD context as early as 1976 [9]. In [10] a comprehensive tutorial on how to derive such a matrix formulation in the scope of WDFs is given. Apart from the loss of circuit topology, another drawback of this method is that a matrix multiplication isn't necessarily passive under finite arithmetic conditions. This can be circumvented by means of a factorization of this scattering matrix which yields a realization that is a composition of two-port Wave Digital elements [11], ensuring passivity even in the presence of round-off errors. Unfortunately, the derivation is quite cumbersome and has to be redone for every minor change in the circuit. An approach that is somewhere in the middle of the road between a classic WDF and a global scattering matrix implementation is presented in [12]: In a first step, as much elements that are connected via serial or parallel connections are successively separated from the rest of the circuit as possible. These subcircuits are easily implemented by means of classic tree-like Wave Digital Filters. Then, the rest of the circuit is consolidated as a so-called $\mathcal{R}$-node, a substructure that is not realizable as a classic WDF and which has to be implemented otherwise, e.g. by means of [10]–[11]. Structures built with this approach typically look like the example circuit shown in figure 4. For a lot of circuits, however, only very small WDF trees can be separated this way, leading to structures where *most* of the circuit is handled as a non-modular scattering matrix. In the simple bridged T circuit in figure 3, for example, the whole structure except for the WD elements (the leaves of the tree) would be contained inside the $\mathcal{R}$-node.

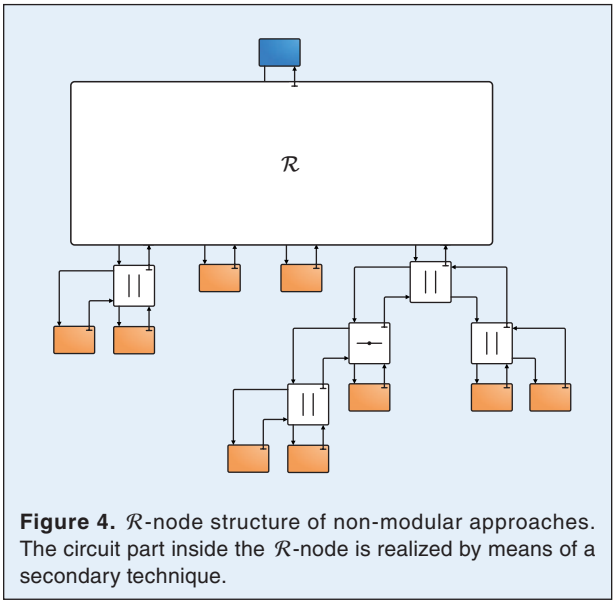

Figure 4. $\mathcal{R}$-node structure of non-modular approaches. The circuit part inside the $\mathcal{R}$-node is realized by means of a secondary technique.

In terms of nonlinear circuits, the basic topological concepts to derive a realizable structure are similar to the linear case. On one hand, there are global descriptions that utilize a state space formulation based on wave variables, e.g. [13]. The nonlinearities are handled in Kirchhoff domain here and need to be solved by means of a Newton iteration at every time step. On the other hand, there are hybrid approaches [14]–[15] as in the linear case that aim to implement as much of the structure by means of classic WDF trees and concentrate the problematic rest of the circuit that doesn't fit into the tree scheme in an $\mathcal{R}$-node which is implemented as above. In addition to the linear approach, all nonlinearities are grouped at that node. To solve the implicit loops at the grouped nonlinearity, either a tabulation technique or, in the general case, again Newton's method is proposed. In the special case of a single one-port nonlinearity, the $\mathcal{R}$-node can be implemented with one reflection-free port that is able to accommodate this nonlinear element as shown in blue in figure 4.

III. A Strictly Modular Solution

"So you've got a delay-free loop that you can't process, why not just put a delay into it?" I hear you say. Well, the idea is not bad at all, as we'll show in the next paragraph.

A. The Contractivity Property

Assume a simple, but non-computable signal flow graph as in figure 5(a). Here, the output y is multiplied by a factor L and fed back to an adder, where a constant a_0 is applied, yielding

$$y = a_0 + L \cdot y. \tag{2}$$

Obviously, the output y appears on both sides of the equation, marking an implicit formulation. If $L \neq 1$, an explicit solution can be found *algebraically*, hence the often-used name *algebraic loop*. In this most trivial case the simple manipulation

$$\begin{aligned} y &= a_0 + L \cdot y \\ \Leftrightarrow\ y &= \frac{a_0}{1-L} \end{aligned} \tag{3}$$

solves the implicit problem. Of course, in terms of a signal flow graph this rearrangement implies a complete reformulation of the topology of the structure, as well. So, to preserve the topology, we try to solve this loop by inserting a delay element as in figure 5(b). This structure is not constant with respect to time anymore, so we denote the current time step by k and assume that for $k \leq 0$, the memory of the delay element is zero. Evaluation of $y(k)$ yields

$$\begin{aligned} y(0) &= a_0 \\ y(1) &= L \cdot a_0 + a_0 \\ y(2) &= L^2 \cdot a_0 + L \cdot a_0 + a_0 \\ &\vdots \end{aligned} \tag{4}$$

which can be written as

$$y(k) = \sum_{i=0}^{k} a_0 L^i \tag{5}$$

for the general case. The right hand side of this familiar looking expression consists of the first $k+1$ terms of the geometric series, which converges if and only if $|L| < 1$. In that case the well-known formula

$$\lim_{k\to\infty} y(k) = \sum_{i=0}^{\infty} a_0 L^i = \frac{a_0}{1-L} \tag{6}$$

holds. So if the absolute value of L is smaller than one, the structure with inserted delay element converges towards the algebraic solution.

But how to generalize this observation to be useful for our Wave Digital Filters? One way to look at it is to interpret the delay as the iteration of a function f. If the output of the delay at time step k is denoted by $w(k)$, we may define

$$f(w(k)) = L \cdot w(k) + a_0 \tag{7}$$

as illustrated in figure 5(c). The behavior of this iteration now is solely dependent on some properties of f, as basically f is applied to its own output over and over again. In case of convergence, the state eventually approaches an equilibrium $\bar{w}$ where

$$f(\bar{w}) = \bar{w}, \tag{8}$$

which is also known as a *fixed point* of f. A very powerful criterion that guarantees convergence is if f is a *contraction*, i.e. if f is Lipschitz continuous with a constant $K < 1$. Intuitively, this means that the absolute of the rate of change is limited by K—in case of a differentiable function, the absolute value of its derivative would not reach or exceed One. For each such contraction mapping, *Banach's fixed point theorem* [16] applies and guarantees that a) there is a fixed point, b) that this fixed point is unique and c) that a fixed point iteration as above always converges towards this fixed point.

In case of our example, the derivative of $f(w)$ is $f'(w) = L$, thus f is such a contraction with guaranteed convergence if $|L| < 1$, mirroring the constraint of the geometric series. Note that in a linear system like this, contractivity is closely related to the stability of the system: For $|L| < 1$, the system is both strictly stable and contractive, for $|L| = 1$ it is marginally stable and for $|L| > 1$ it diverges, never approaching the fixed point in the latter cases.

B. Are WDFs Contractive?

Alfred Fettweis was aware that fixed point iterations are able to solve a number of realizablity issues [17] in WDFs and other authors in the field used iterative approaches as well [18]. But when can we expect convergence? Are WDFs contractive?

To answer this question systematically, we are going to concentrate on linear WDFs first. As we have seen, the contractivity property is closely related to the stability of the

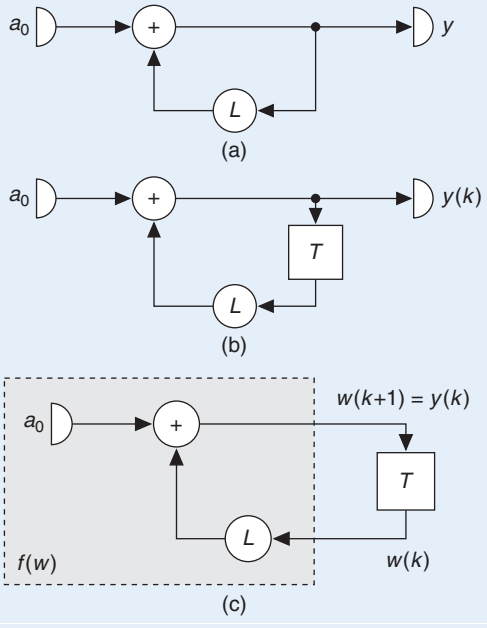

Figure 5. Example: Resolving an implicit loop. (a) Implicit description containing an algebraic loop. (b) Explicit iterative description. (c) Description as fixed point iteration.

Iteration can solve any wave-based delay-free loop in passive linear WDFs with guaranteed convergence, be it local or macroscopic.

linear system. In terms of stability of linear WDFs, we already know that our system is passive, which is a very powerful statement as it ensures that the total energy at the output cannot exceed the total energy at the input, thus it guarantees that no divergence takes place. Unfortunately, we still don't know what happens within the system's states at all.

To shed some light on that matter, in [19] a normal form for linear Wave Digital Filters is introduced. It can be shown that any power wave WDF that only has resistive sources (as opposed to idealized sources) can be described as a system $\mathcal{S} = (\mathbf{A}, \mathbf{B}, \mathbf{C}, \mathbf{D})$ with a state space representation

$$\begin{aligned} w(k+1) &= \mathbf{A} \cdot w(k) + \mathbf{B} \cdot x(k) \\ y(k) &= \mathbf{C} \cdot w(k) + \mathbf{D} \cdot x(k), \end{aligned} \tag{9}$$

with $\mathbf{A} \in \mathbb{C}^{m \times m}$, $\mathbf{B} \in \mathbb{C}^{m \times n}$, $\mathbf{C} \in \mathbb{C}^{n \times m}$ and $\mathbf{D} \in \mathbb{C}^{n \times n}$, where the associated scattering matrix

$$\mathbf{S} = \begin{pmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{pmatrix} \in \mathbb{C}^{\ell \times \ell}, \qquad \ell = m + n \tag{10}$$

is unitary, thus

$$\mathbf{S}^* \mathbf{S} = \mathbf{I}. \tag{11}$$

In this notation, the state vector is denoted by w, while x and y are input and output, respectively, the asterisk "$*$" denotes the conjugate transpose and $\mathbf{I}$ is the identity matrix. Now, with this definition as a unitary filter (or orthogonal filter in the real case, c.f. [20]), the stability of WDFs can be analyzed systematically. Here, the above system is strictly stable iff the spectral radius of $\mathbf{A}$ (the largest absolute eigenvalue) $\rho(\mathbf{A}) < 1$ is smaller than One. In our case, an equivalent statement is that the system is strictly stable iff the spectral norm (the largest singular value) $\|\mathbf{A}^m\|_2$ of $\mathbf{A}^m$, the m-th power of $\mathbf{A} \in \mathbb{C}^{m \times m}$, is smaller than One, thus

$$\|\mathbf{A}^m\|_2 < 1. \tag{12}$$

Note that the choice of the m-th power of $\mathbf{A}$ is only possible because $\mathbf{A}$ is a submatrix of a unitary matrix and thus all singular values are no larger than unity[1].

[1]In fact, there are 'lossy' singular values smaller than unity on the one hand and 'lossless' singular values equal to One on the other. If there is a vector v that does not undergo dissipation in p-fold application of $\mathbf{A}$, thus $\|\mathbf{A}^p v\|_2 = \|v\|_2$, all smaller powers $\mathbf{A}^q v, q = 0,\ldots,p-1$ must have been mapped onto lossless singular values exclusively. Since $\mathbf{A}$ is an $m \times m$ matrix, if losslessness holds for $p = m$ steps, the Cayley-Hamilton theorem suggests that all higher powers of $\mathbf{A}$ won't introduce losses for this particular vector v either, contradicting strict stability. Obviously, this criterion does not apply to the general, non-passive case with singular values exceeding One. Full proof in [19].

The latter, alternative criterion comes in handy here, as it describes the time step when the actual dissipation takes place and, more importantly, as a matrix norm formulation it is quite easy to extend to the nonlinear case.

Based on these definitions, a number of results are obtained in [19] that describe the system state of a Wave Digital Filter more closely:

- WDFs in normal form are strictly stable if and only if they are observable.
- The observability of a WDF in normal form is equivalent to its controllability.
- If a WDF in normal form is not observable/controllable, it always can be partitioned into two disjoint subsystems, where one is observable, controllable and strictly stable, and the other is lossless and not connected to both input and output.
- WDFs in normal form are BIBS (Bounded Input $\Rightarrow$ Bounded State) and BIBO (Bounded Input $\Rightarrow$ Bounded Output) stable.

As a direct result of these stability properties, it is shown in [19] that linear WDFs are indeed contractive, although not necessarily for every time step, but at the latest after m steps, where m is the number of states[2]. This is because in some circuits energy is shifted back and forth between reactive elements before finally arriving at a resistance. Here, dissipation takes place that forces the ratio of remaining stored energy to applied energy to drop below the Lipschitz constant $K < 1$. A simple example for this behavior is a damped LC resonator circuit [19]. Fortunately, this makes no difference for the application of Banach's theorem, as there is a variant that is defined for the m-th power of a mapping [22]. So now we know that iteration is able to solve any wave-based[3] delay-free loop in linear WDFs with guaranteed convergence, be it local or macroscopic.

C. Iteration Scheme

Assume a WDF that is constructed to emulate an analogue filter circuit like the bridged T circuit in figure 3 that would suffer from non-computable delay-free loops if implemented directly. To make it work, we just have to insert a delay into that loop and are ready to start the

[2]Note that this is a much more precise and general statement than the initial assumption of the authors in [21], which is true for WDFs with a *symmetrical* global scattering matrix.

[3]The choice of wave definition does not make any difference here and the findings apply to voltage waves equally.

simulation, right? Not quite. All we know up to now is that a proper fixed point iteration is guaranteed to converge, not that a simple delay will do the trick. The problem to be aware of here is the presence of other delay elements in the circuit that mimic the reactive behavior of capacitors and inductors. So we have to be careful not to impair the dynamic characteristics of the structure along time axis with our iteration approach. The most simple and practical way to do so is by introducing a second, *artificial time axis* t_2 that takes care of the iteration for any instant in *factual time* t_1. This way, we can define delay elements in t_2 direction that deal with the implicit loops, while iterating the memoryless part of the circuit only to decouple iteration memory from the real system's state inside of capacitors and inductors. This decoupling is needed to suppress unwanted multidimensional dynamics and is realized by holding the output values of reactive elements (the t_1 delays) constant along the iteration.

With these definitions, a proper Wave Digital Filter realization of the bridged T example looks like the structure shown in figure 6 (from [21]). The fixed point iteration is handled by the iteration elements denoted by T_2, while the system state stored inside the capacitors is implemented separately by the T_1 delays in t_1 direction. This multidimensional notation makes the adaption of other reference circuits very easy while maintaining the property of guaranteed convergence. Note that with this method, the resulting WDF has the same topology as the analogue reference circuit (shown in figure 3 for this example) and features all circuit elements explicitly. This means that virtual measurements can be taken at any wave port and reflect the respective Kirchhoff quantities at that port in the reference circuit.

At each time step, the iteration is stopped when the absolute difference between two iteration steps drops below a given threshold, i.e. if the inputs and outputs of the delay elements are *almost* the same, thus are a good approximation of the fixed point $\bar{w}$ from equation (8).

D. Nonlinear Elements

With the findings above, we already found a way to solve the topological constraints the classic WDF approach suffered from. Fortunately, the extension of the method towards modelling of nonlinear circuits is quite straight forward: The composition of two contractions gives another contractive map, no matter whether we're composing linear or nonlinear functions. For our Wave Digital Filters this means that we can take our linear base circuit and apply an arbitrary number of contractive nonlinearities via iteration elements without compromising convergence of the iteration. The most prominent example of contractive nonlinear Wave Digital elements is without doubt the simple Shockley diode [23]. Note that contractivity is a stronger property than incremental (or local) passivity (c.f. [24]), as the lossless condition is strictly excluded: A Shockley diode is incrementally passive, dissipative and contractive in WD domain. In contrast, an ideal diode is incrementally passive but lossless and corresponds to a so-called nonexpansive map that even might prevent convergence if in composition with a contractive linear WDF [19].

Even if the nonlinearity is not contractive but does contain an 'active' region that can be used for amplification purposes, the fixed point iteration may converge towards the correct solution. Obviously, Banach's theorem can't be applied in this case, which is reflected intuitively by the fact that with such a device even unstable circuits can be built, so the surrounding circuitry has to be taken into consideration as well. There is a somewhat weaker statement called Ostrowski's theorem [25] that can be applied here: Assume that the nonlinear function that is a composition of said noncontractive elements and the memoryless circuitry they are embedded into has a fixed point $\bar{w}$. If the Jacobian of that composition has a spectral radius smaller than One in a neighborhood around $\bar{w}$, each fixed point iteration starting in that neighborhood will converge towards $\bar{w}$.

For cases where pure fixed point iteration does not suffice, a damping of the iteration can be applied ([18], proof in [19]) which effectively reduces the iteration step size. Another technique is to adapt the iteration step size dynamically to the nonlinearity [26], utilizing a local approximation of Newton's method. A highly nonlinear example circuit is presented in section V which relies on the latter approach but does converge likewise, albeit slower, with a pure fixed point iteration as well.

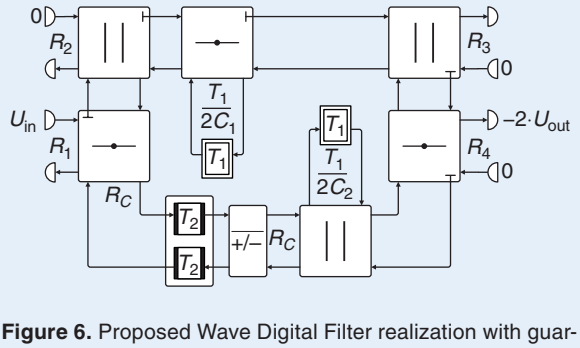

Figure 6. Proposed Wave Digital Filter realization with guaranteed convergence of the bridged T circuit in figure 2. Modified delay elements T_1 correspond to the reactive elements of the circuit. Delay elements T_2 implement the fixed point iteration, while T_1 is held constant. The block denoted with $\overline{+/-}$ compensates for the sign mismatch shown in figure 3 by switching polarity.

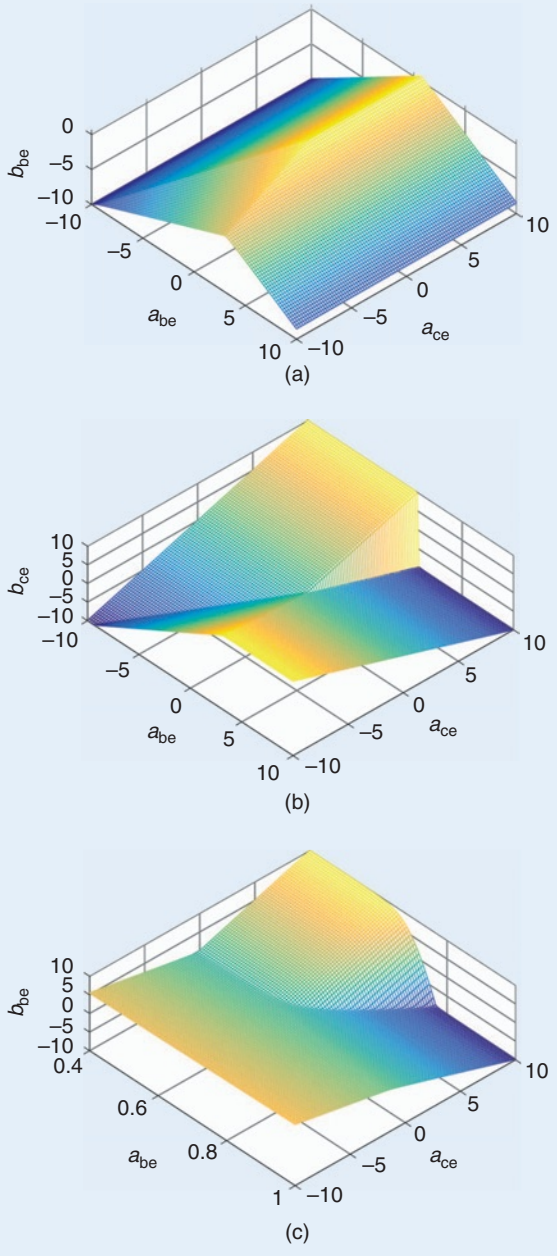

Figure 7. Nonlinear wave model of bipolar junction transistor. (a) & (b) Tabulation result with proposed approach, (c) detail on non-contractive region of the collector-emitter junction. If the transistor is wired in an amplifier configuration, this is, by design, where the operating point is located. (a) Proposed result of the reflected wave b_{be} at the base-emitter junction. (b) Proposed result of the reflected wave b_{ce} at the collector-emitter junction. (c) Proposed result of the reflected wave b_{ce} at the collector-emitter junction (zoomed in on 'active' region).

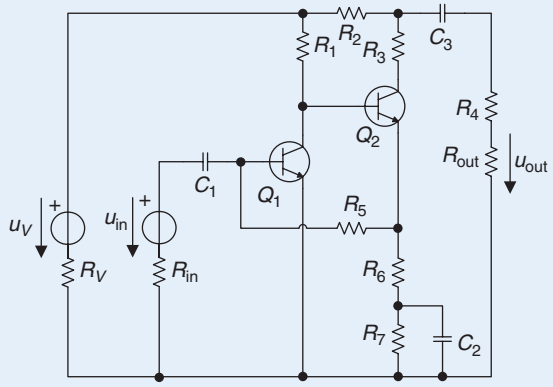

Figure 8. 'Fuzz Face' circuit in Kirchhoff domain.

IV. Modelling of Nonlinearities

In the following, we're having a look at how to derive new nonlinear device models in Wave Digital domain, shown by example of a bipolar junction transistor (BJT). As pointed out earlier, the classic Wave Digital Filters were not able to accommodate multi-port nonlinear elements like transistors at all, so it comes as no surprise that there isn't a lot of research on how to describe such elements in terms of wave variables. In fact, a lot of simulations in the literature involving nonlinear elements use the underlying Kirchhoff definition of the nonlinearity itself, i.e. a direct functional voltage-current relationship. The reasoning behind this change of domain is that for most practical cases there simply is no closed form solution to the transformation of the Kirchhoff nonlinearity (like $i = f_{\mathrm{KH}}(u)$) into wave domain ($b = f_{\mathrm{WAVE}}(a)$) by applying equation (1). Even in quite simple cases like a Shockley diode, the derivation of functional approximations becomes cumbersome [27]. Because of that, the most often used technique here is to realize the coordinate transformation on a point-wise basis, tabulate the transformed values and interpolate in between at runtime. Unfortunately, even this is not as straight forward as expected: Common techniques like the Newton method diverge easily because of the demanding definitions of some nonlinearities in Kirchhoff domain. For example, if the Ebers-Moll model for bipolar transistors [28] is to be evaluated within a range of just a few volts, the requirements to numerical dynamic range are quite extreme, as mostly exponentials are involved. Even with double precision floating point data types, proven tools like Matlab's *fzero()* struggle to converge towards the solution. The function is able to converge with the help of very close initial guesses only, meaning a priori knowledge of the solution that obviously is not available at this point.

So, to obtain a nonlinear wave representation anyhow, a problem-specific method is proposed in [19] that exhibits a very high numerical robustness and is guaranteed to converge. Instead of trying to solve an implicit equation to obtain the reflected wave quantity b for a given input wave a, the basic idea of the new approach is to generate a big

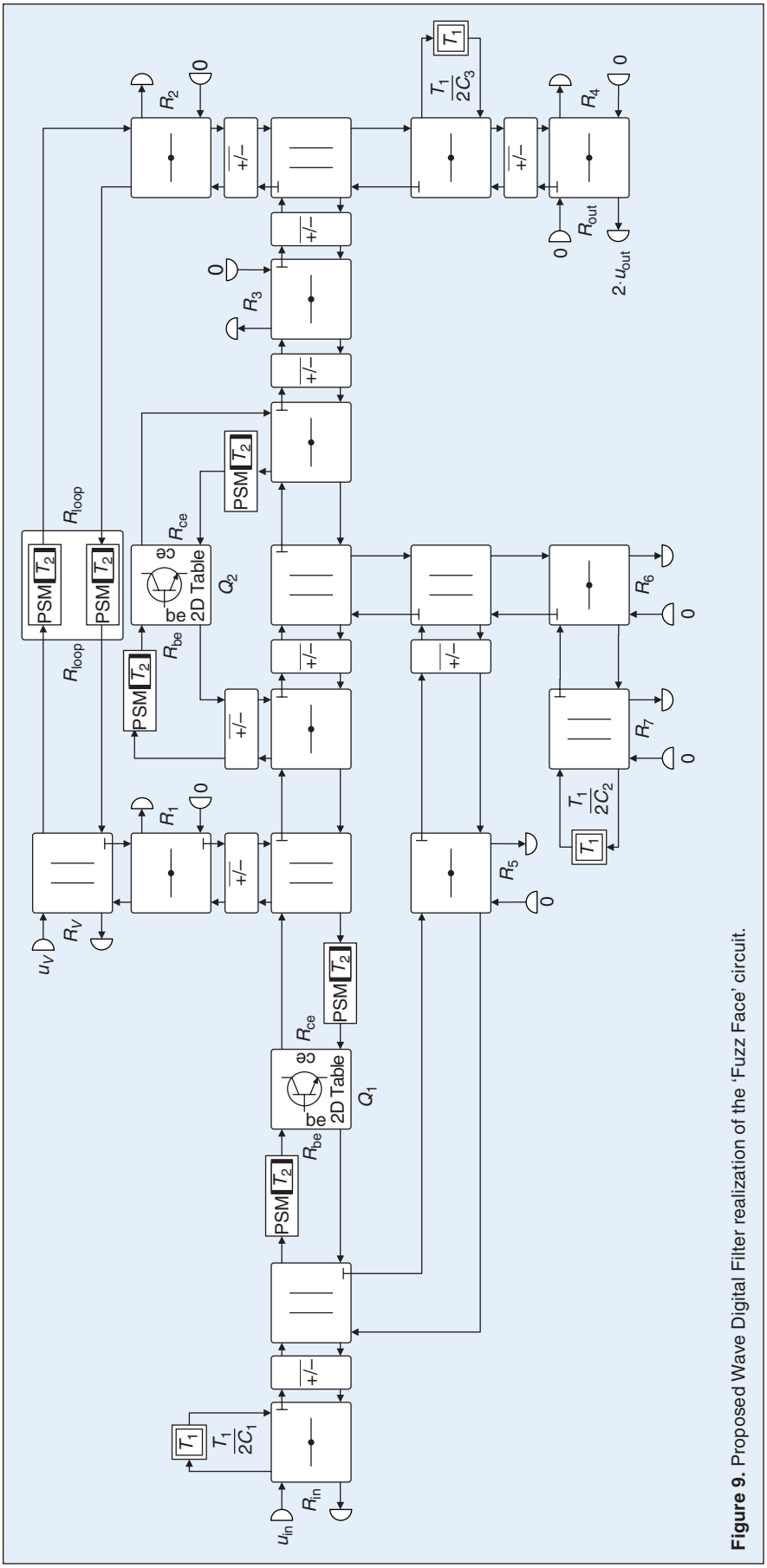

Figure 9. Proposed Wave Digital Filter realization of the 'Fuzz Face' circuit.

point cloud of point pairs (u_p, i_p) that incorporate the nonlinear function which defines the element in Kirchhoff domain, e.g. $i_p = f_{KH}(u_p)$ in case of a voltage controlled nonlinearity. Each of these point pairs is now transformed into its corresponding pair (a_p, b_p) of wave quantities by direct application of the wave definition in (1), yielding a 4-tuple (u_p, i_p, a_p, b_p) of corresponding values that are accurate up to the numerical precision limits of the computer system used. Of course, the loci of the Kirchhoff variables are mapped nonlinearly into wave domain by this procedure, wherefore a relatively large number of points has to be generated to make sure the point density is sufficiently high throughout the region of interest. Finally, these scattered, but extremely accurate points are interpolated linearly to obtain a uniformly spaced table. This interpolation step introduces an approximation error that is bounded by the convex hull of the neighboring correct points, thus by generating more breakpoints the absolute error can be regulated easily. More importantly, by design, there are no issues with non-convergence to be expected. In figure 7(a) and 7(b) the results of the proposed approach are shown for the reflectances of base emitter and collector emitter junctions of a BJT, respectively. The nonconctractive or 'active' region of the transistor is shown enlarged in figure 7(c), highlighting the smooth transition to saturation. To obtain amplifying behavior, the transistor is typically biased so that the operating point lies well within that region. Then, small changes

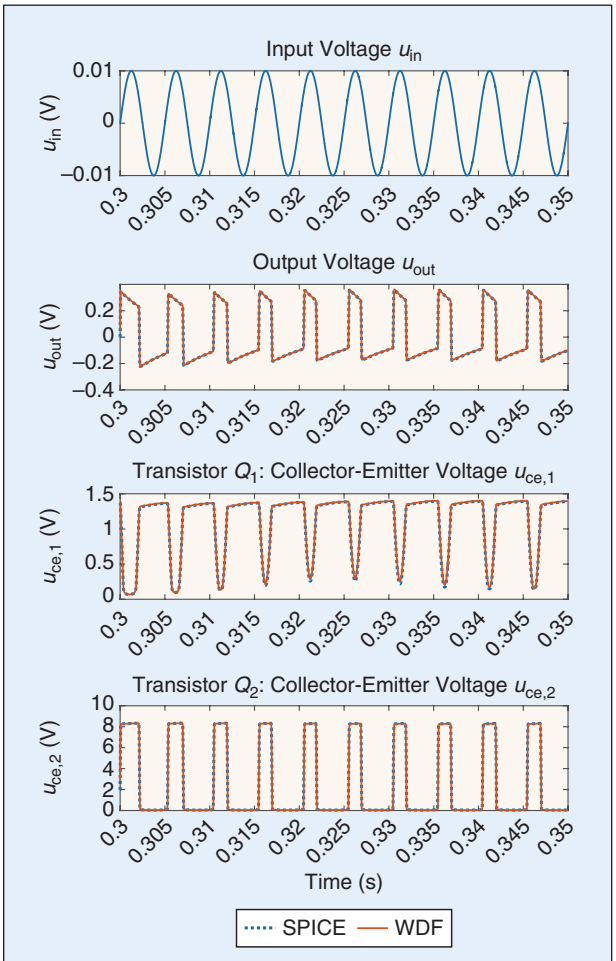

Figure 10. Simulation results of the 'Fuzz Face' Wave Digital Filter realization in comparison to a SPICE reference. From top to bottom: Sine input (200 Hz) and corresponding output signals of the circuit. All internal states are modeled accurately, shown for collector-emitter voltages at the first and second transistor, respectively (bottom plots).

of the a_{be} wave port (the base emitter junction) yield large changes at the b_{ce} port (the collector emitter junction).

V. An Example: The Fuzz Face Circuit

Attracted by the real-time capability of Alfred Fettweis' concept, the musical audio community was one of the main driving forces to extend the theory of Wave Digital Filters towards general nonlinear circuit simulation in at least the last decade [8], [10], [14], [15], [27], [29]. So to give an example circuit that incorporates our findings, let's have a look at a highly nonlinear audio circuit that previously could not be modeled as a Wave Digital Filter at all: The "*Fuzz Face*", introduced by Arbiter Electronics in 1966, is a distortion device for electric guitar that has influenced important recordings of that era like [30] and has become a classic among guitar players ever since. The circuit contains a simple amplifier stage that consists of a pair of npn bipolar transistors[4] with feedback and is depicted in figure 8 (for the component values used please refer to [19]). This Fuzz Face has a lot of gain and a typical guitar input signal is able to drive it into massive, almost rectangular saturation, producing the well-known buzzy "fuzz" sound. For a WDF simulation this circuit is challenging, as a direct implementation would be violating the classic construction principles both in terms of topology (several macroscopic loops) and number of nonlinear ports (a pair of two-port nonlinearities). In figure 9 the proposed extensions of the Wave Digital concept are applied and yield a realizable WDF. The blocks named *PSM* (Pseudo Secant Method) represent a further refinement of the approach and realize a local approximation of the Newton iteration to adapt step sizes of the iteration dynamically [26]. The results are almost identical to a reference simulation with SPICE as depicted in figure 10, where all internal states are emulated faithfully and take a mean of 21.9 iterations per sample step to fall below an error threshold of $\epsilon = 10^{-5} V$. Slight residual differences are a consequence of the different transistor model used in SPICE which features additional effects like parasitic resistances that can't be turned off in simulation.

VI. Conclusion

More than 45 years after Alfred Fettweis first introduced the Wave Digital Filters, the concept is still compelling due to its elegance and its natural connection to scattering matrix theory. More so, recent advances extend the theory towards a universal circuit simulation technique. The presented modular approach is guaranteed to solve all topological constraints in a plug and play manner and can accommodate, in its current state of development, a wide array of nonlinear elements like transistors and diodes already. Of course, there is still a lot of room for refinements and future research, but compared to the de facto standard for circuit simulation SPICE, a few advantages become apparent: In contrast to SPICE, the complexity of WDFs is not determined by the *square* of the number of nonlinearities but is *linearly* proportional to the number of elements used. This seems to hold for the presented iterative extension of the method as well, as a further addition of nonlinearities does not necessarily increase the number of iterations needed. Here the WDF approach might have a general advantage for large scale circuit simulation. Regarding the iteration length, the deciding factor here is the stiffness of the circuit, which in most instances is conditioned favourably by the sole switch to a wave domain description. Because of that and the general passivity of

[4] In the original release, the Fuzz Face was built with pnp germanium transistors and inverted voltage supply. This was changed later as silicon transistors became commercially available.

WDFs, robustness is an inherent property of Wave Digital Filters that SPICE successively acquired over time.

Tim Schwerdtfeger received the B.Sc., M.Sc. and Dr.-Ing. degrees from the University of Wuppertal, Germany, in 2008, 2010 and 2016, respectively. From 2010 to 2017 he was a research associate at the Faculty of Electrical, Information and Media Engineering at the University of Wuppertal with a specialization in both Nonlinear and Multidimensional Wave Digital Filters. Currently, he is working in the field of digital signal processing and mapping of LIDAR data for automotive applications. His research interests include audio signal processing, Wave Digital Filters, circuit theory, image processing, probabilistic filtering and recent machine learning approaches.

Anton Kummert received the Dipl.-Ing. (FH) degree in electrical engineering from the Fachhochschule Coburg, Coburg, Germany, in 1982, and the Dipl.-Ing. and Dr.-Ing. degrees from the Ruhr-Universität Bochum, Bochum, Germany, in 1985 and 1988 respectively. From 1985 to 1991, he was a Research Assistant at the Department of Electrical Engineering of the Ruhr-Universität Bochum. From 1991 to 1995, he was employed by STN Atlas Elektronik, Bremen, Germany. Since 1995 he has been a professor for Communication Theory at University of Wuppertal, Wuppertal, Germany. Currently he is Dean of the Faculty of Electrical, Information and Media Engineering. Dr. Kummert is a recipient of the Heinrich-Kost-Preis (1989) and of the Akademie-Preis of the Rheinisch-Westfälische Akademie der Wissenschaften (1990). He is a member of VDE, ITG and Senior member of IEEE. He is and has been member of the editorial board of several international journals, organizer and chairman of numerous sessions at major conferences, and one of the General Chairs and organizers of the 4th Int. Workshop on Multidimensional (ND) Systems. He is Editor of the journal Multidimensional Systems and Signal Processing. His current research interests comprise multidimensional systems and circuit theory, image processing and generation, wireless ad hoc networks, tomographic reconstruction methods, artificial intelligence and machine learning.

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